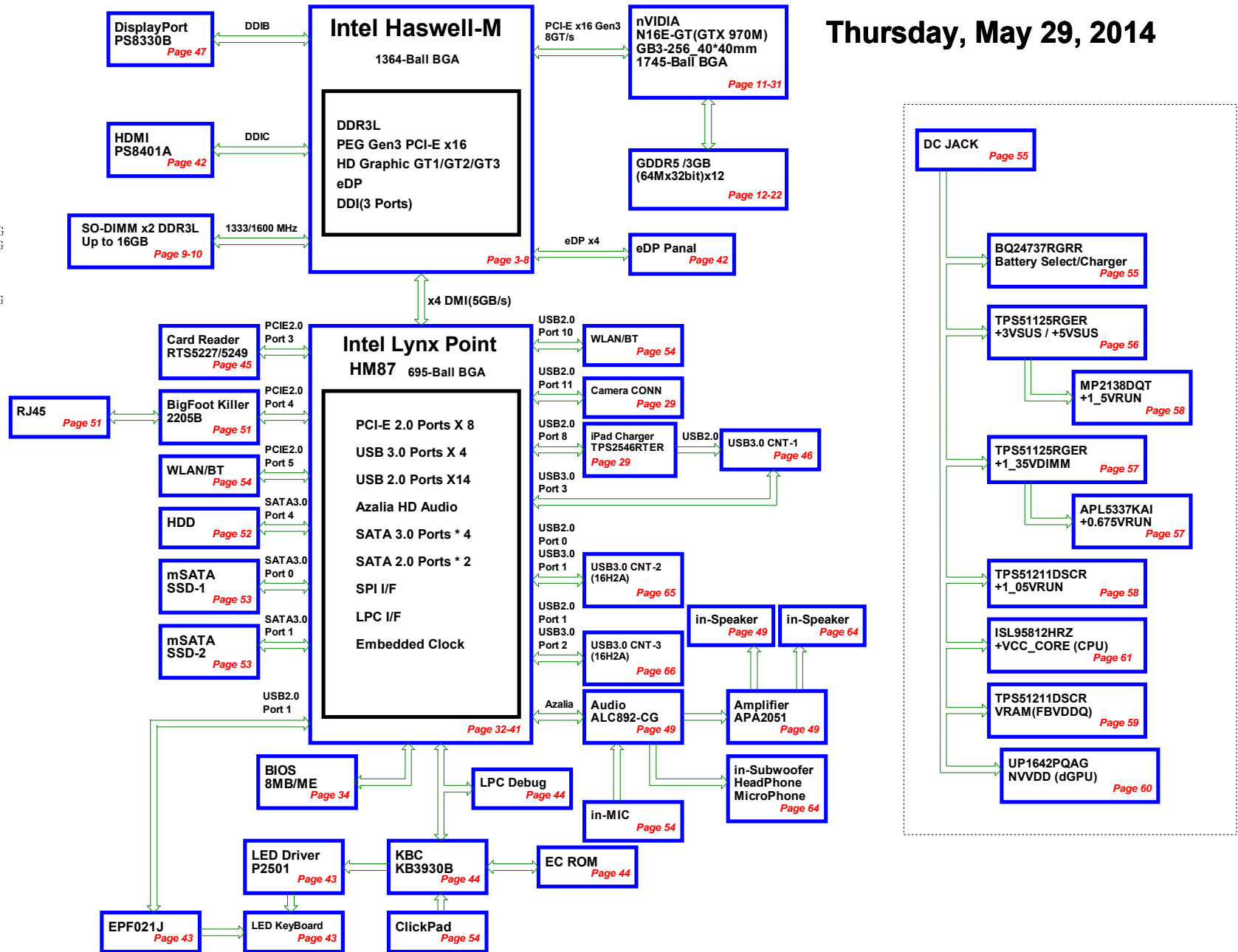


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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVDD	V Core Voltage for nVIDIA dGPU	NVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVDD_EN

Net Naming Conventions

Suffix

= Active Low Signal

Prefix

H = Host

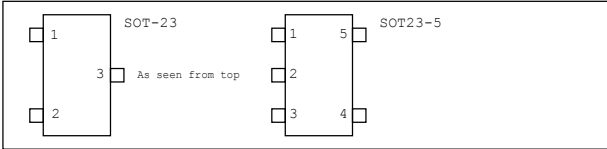
M = DDR Memory

TP = Test Point (does not connect anywhere else)

FB = DGPU VRAM

VIAxxx = Like Test Point, but using VIA.

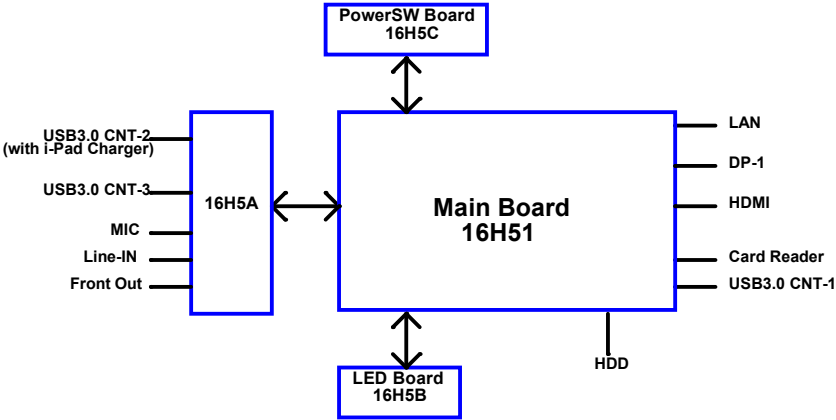
PCB Footprints



POWER STATES

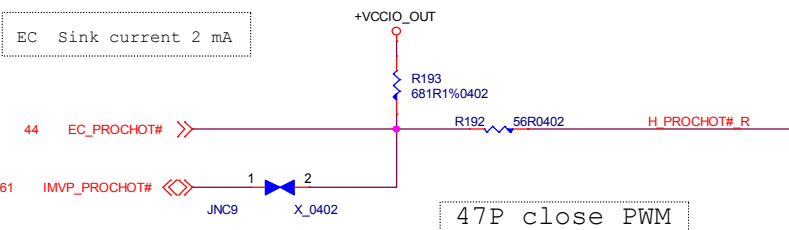
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high



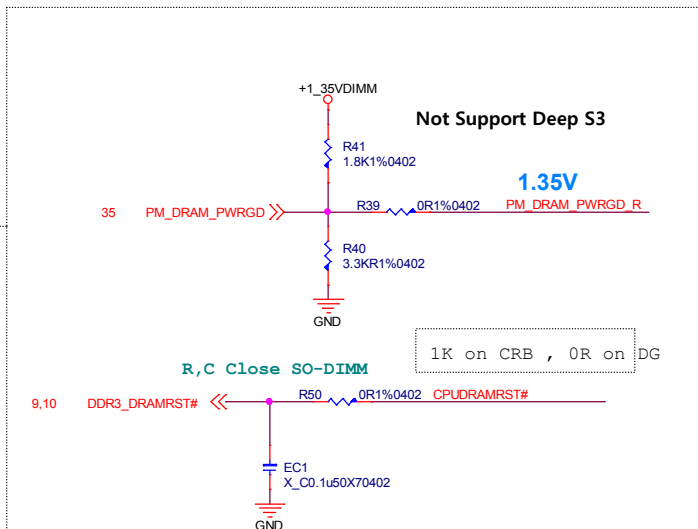
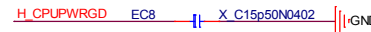
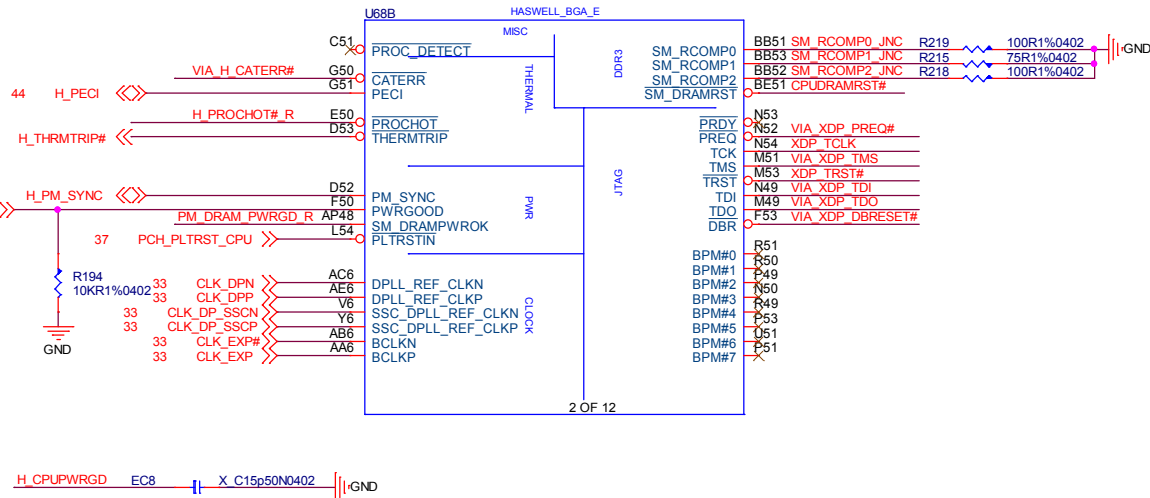
Haswell (DMI,PEG,FDI)

PEG RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

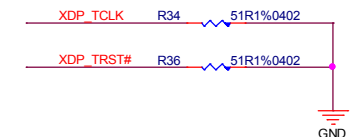


Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil



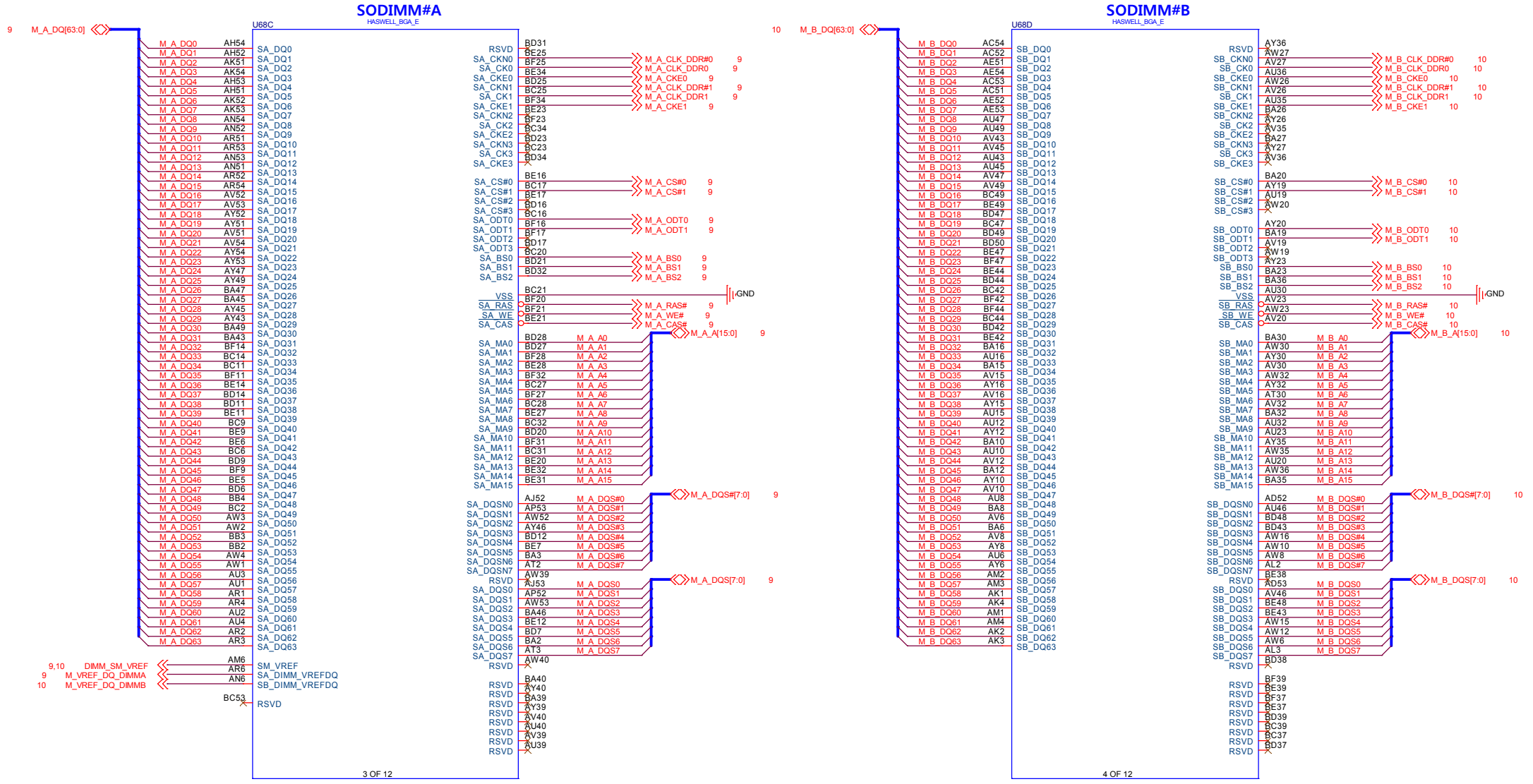
p.11 479493 479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.



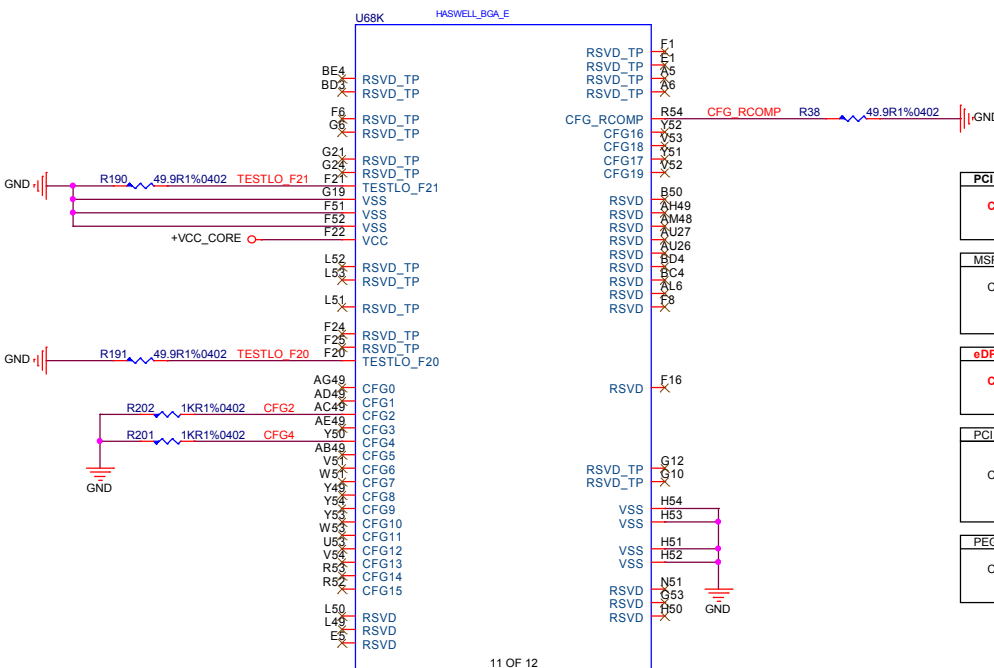
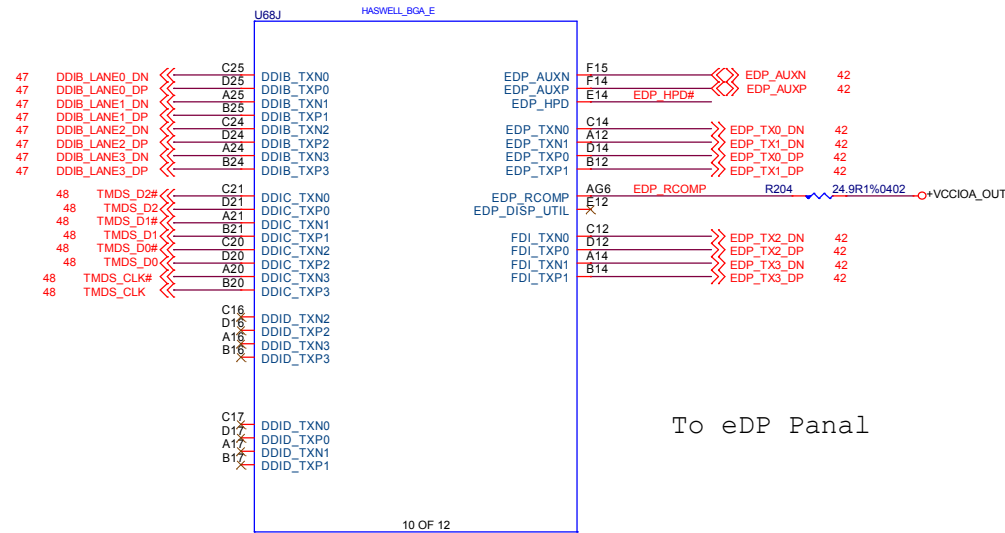
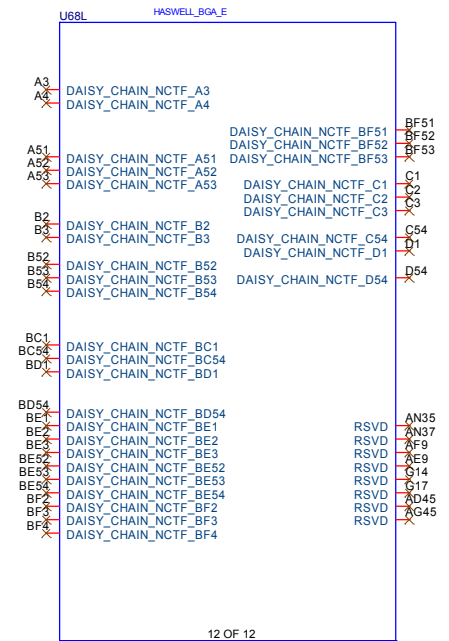
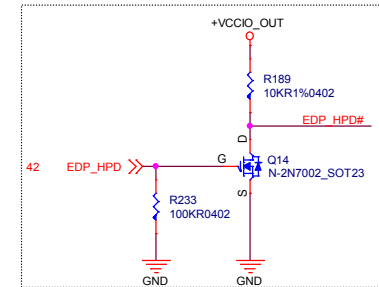
msi MICRO-STAR INT'L CO.,LTD.

Title: **CPU-1 (Host Bus)**
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Haswell (DDR3L)



To eDP Panel



PCI Express® Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

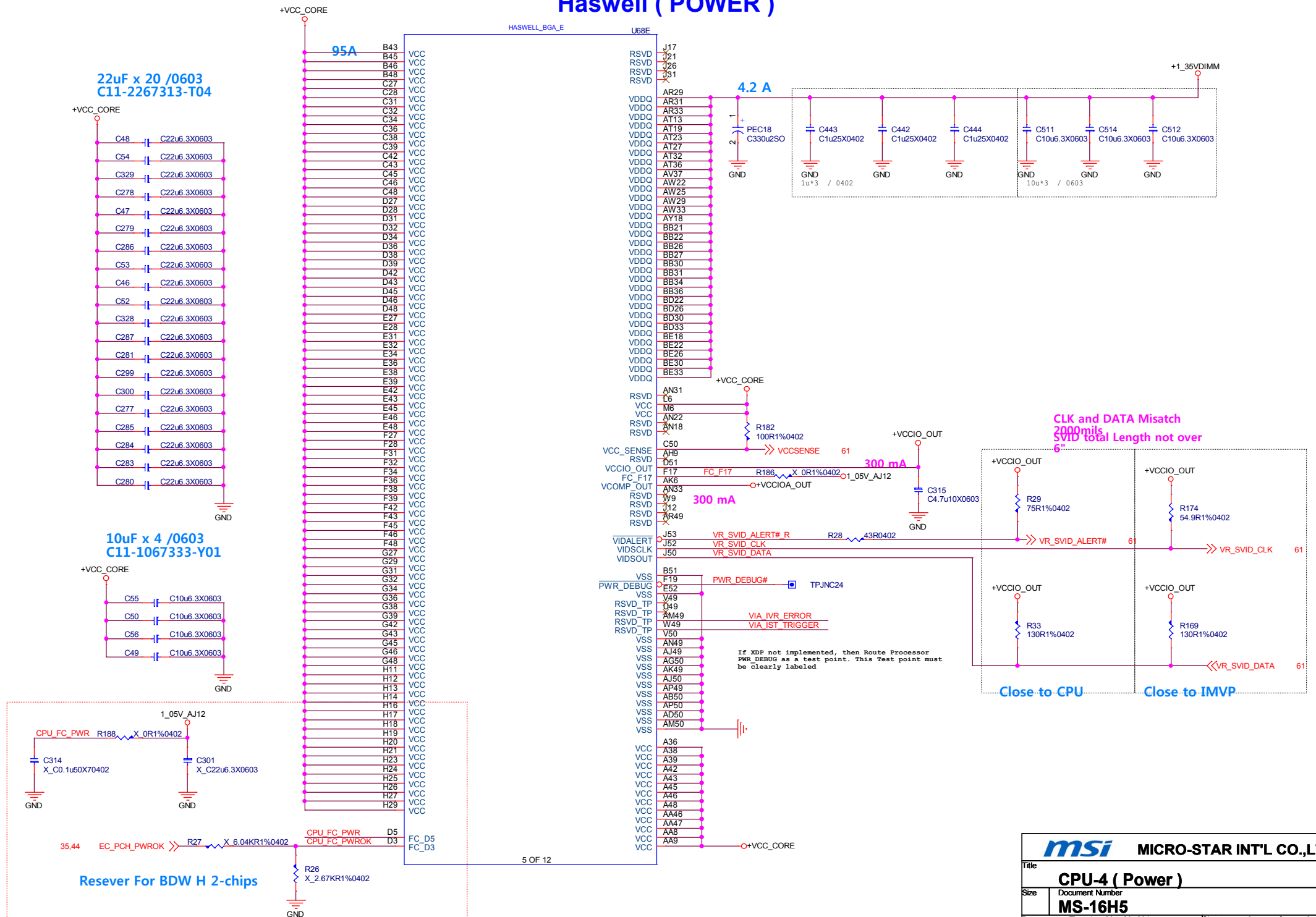
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

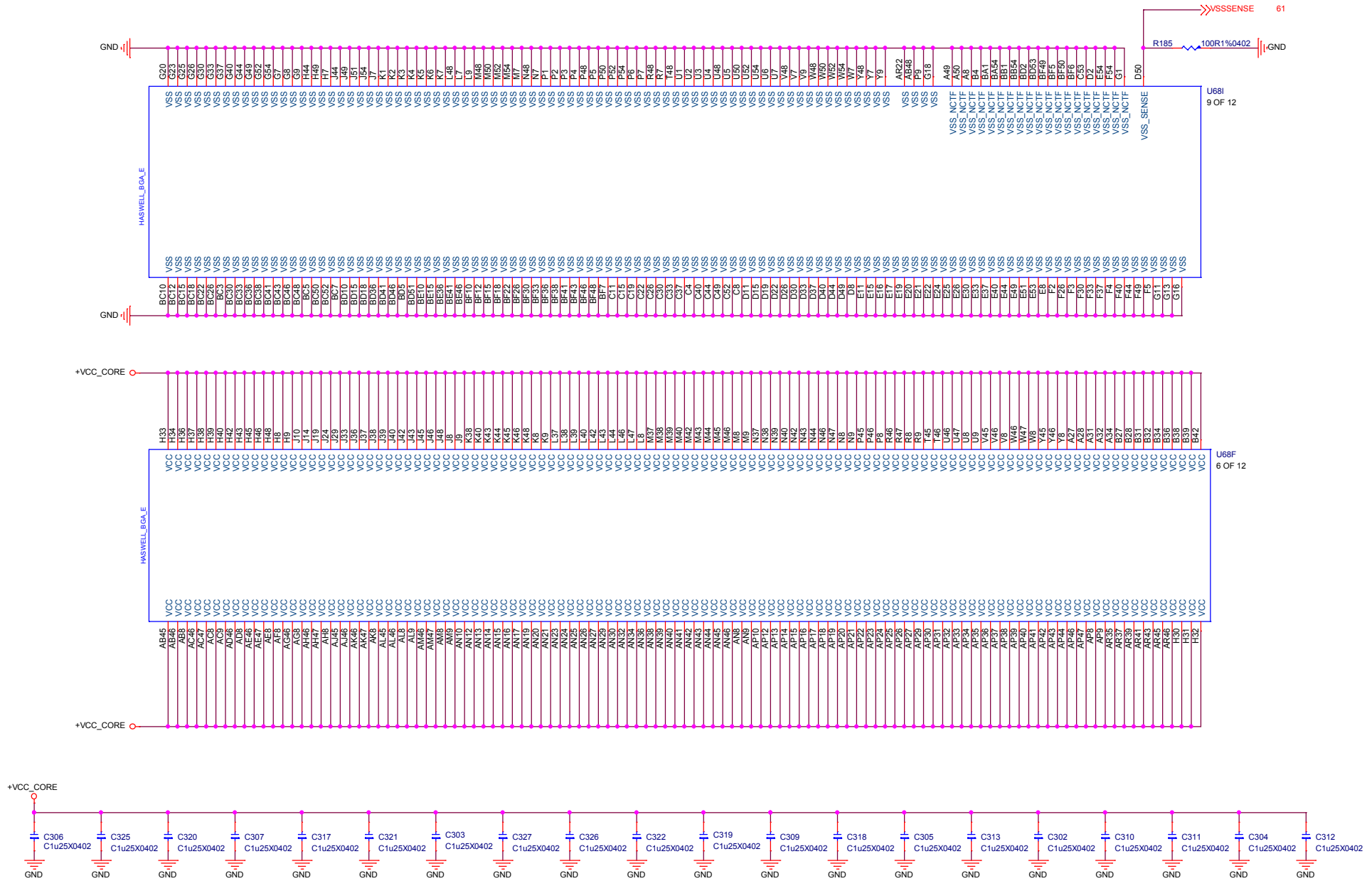
PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

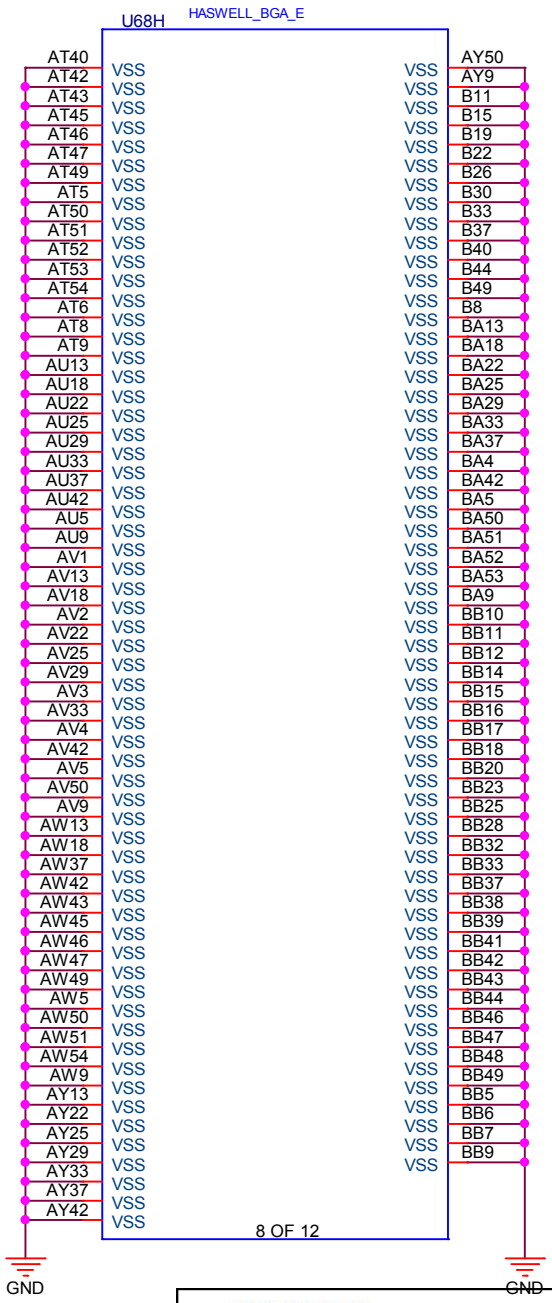
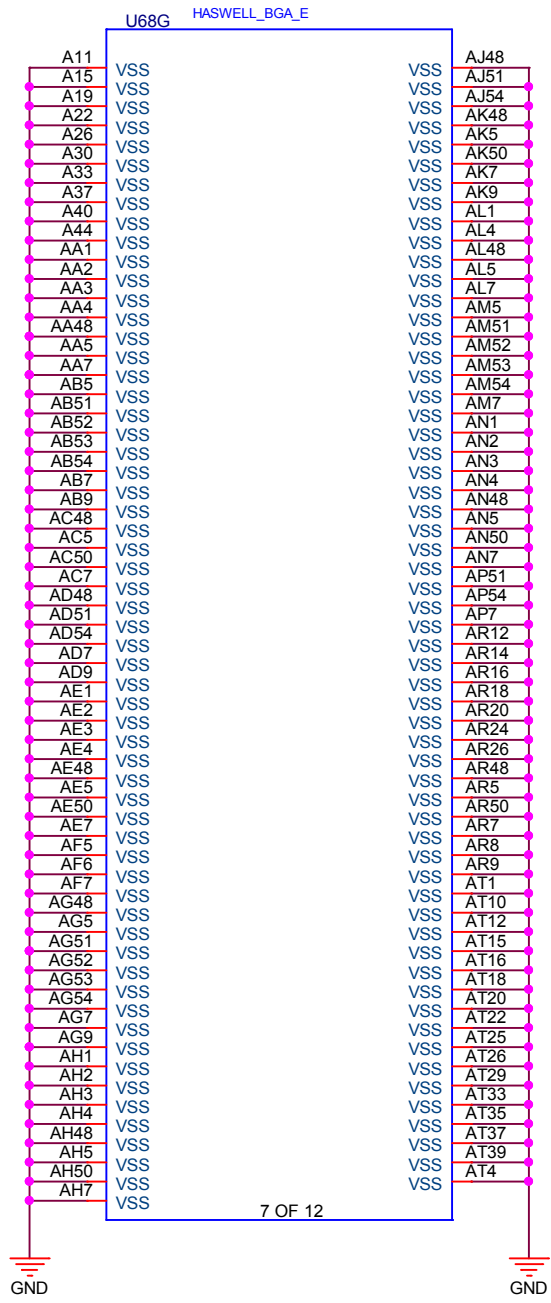
Haswell (POWER)




Haswell (Power & GND)



Haswell (GND)

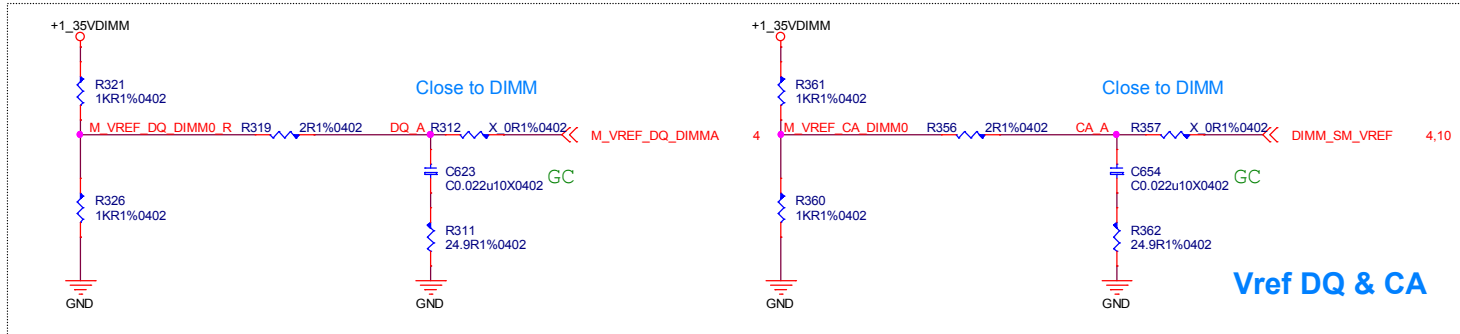
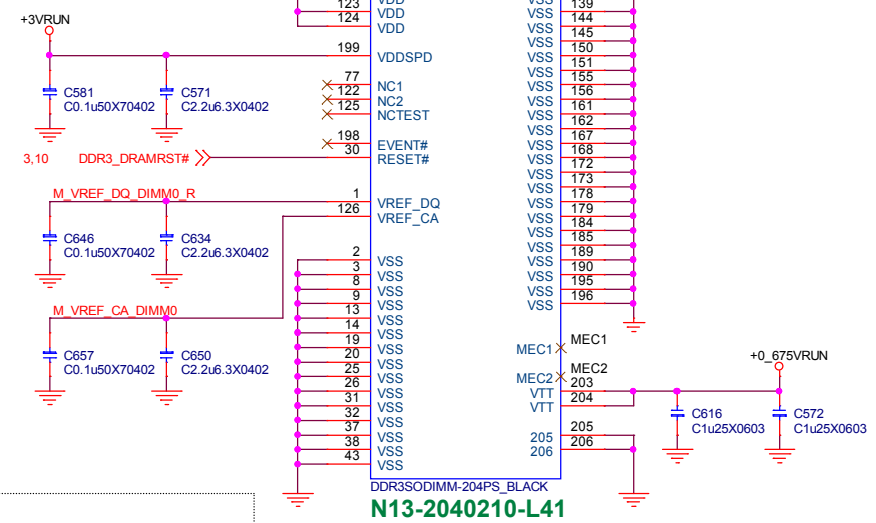
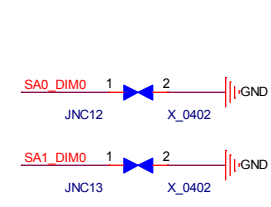
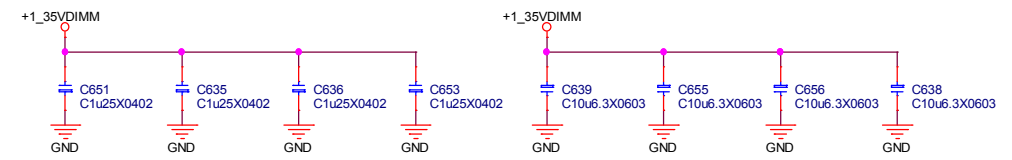
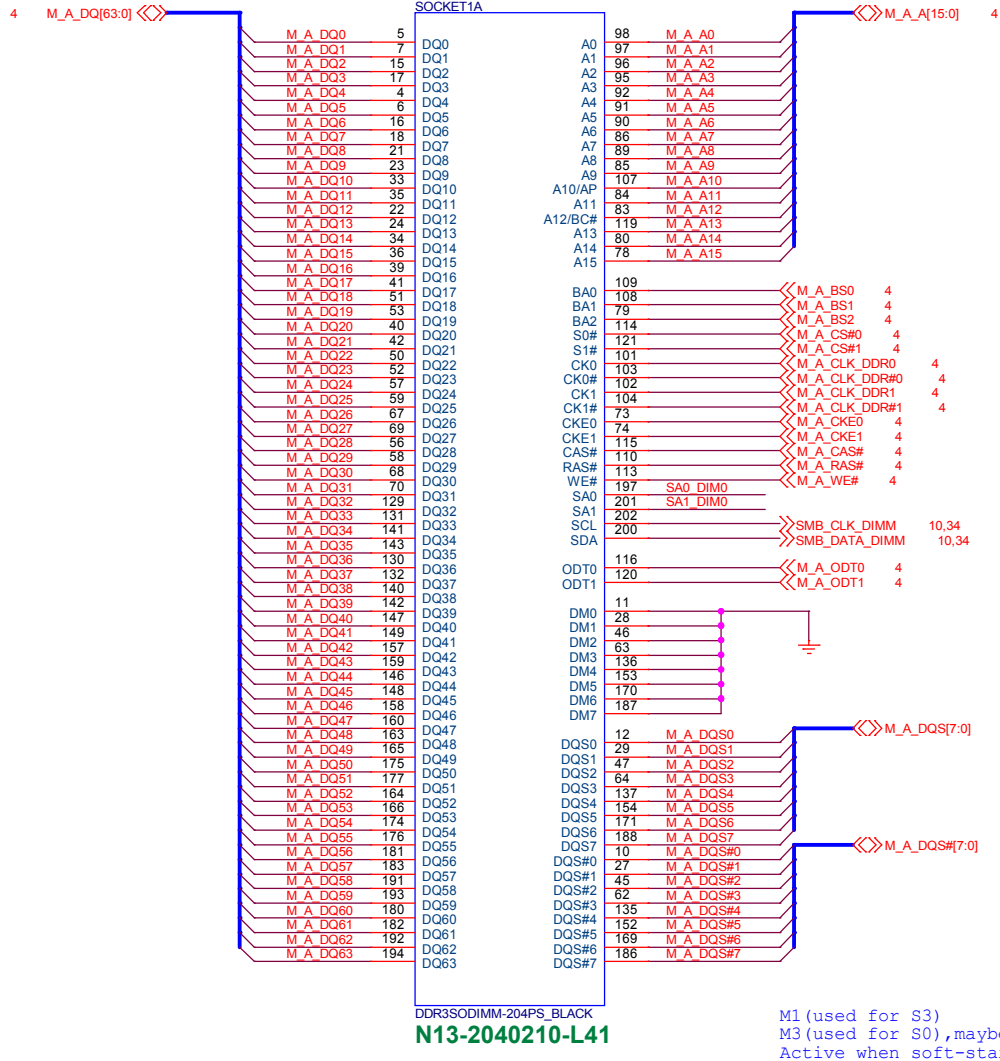




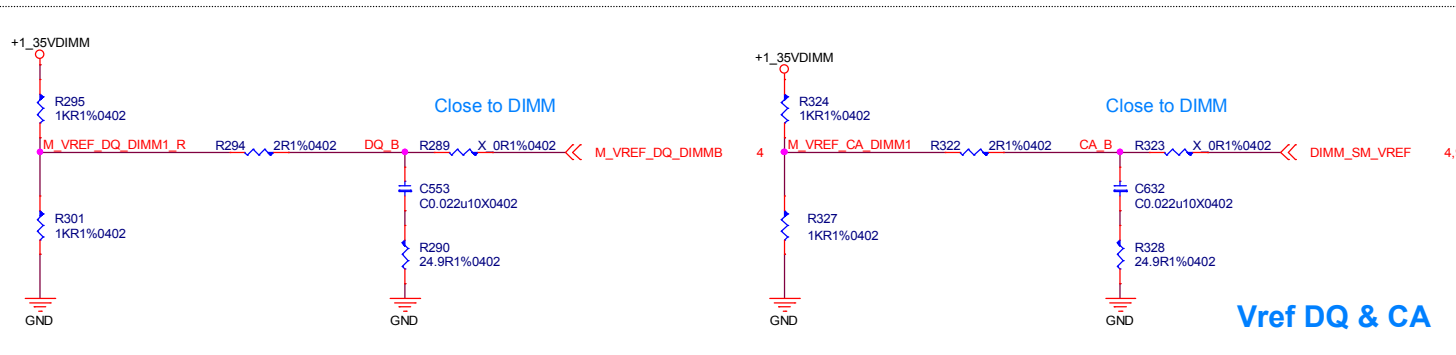
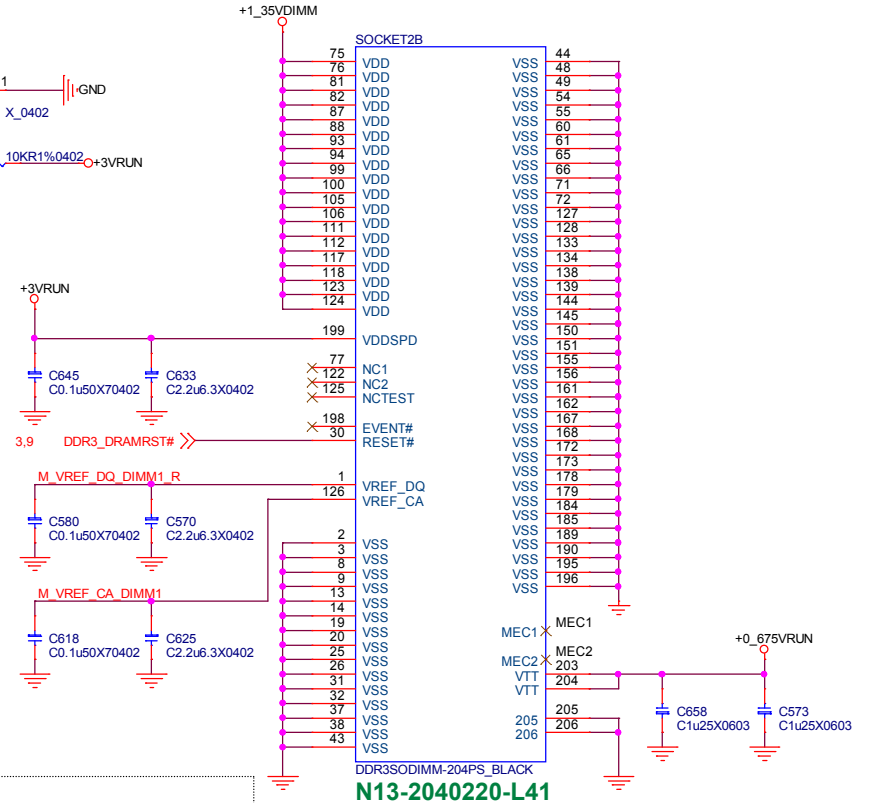
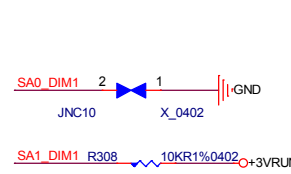
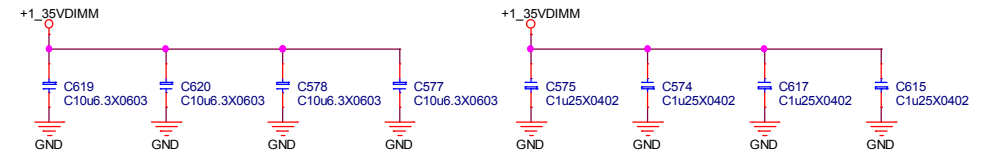
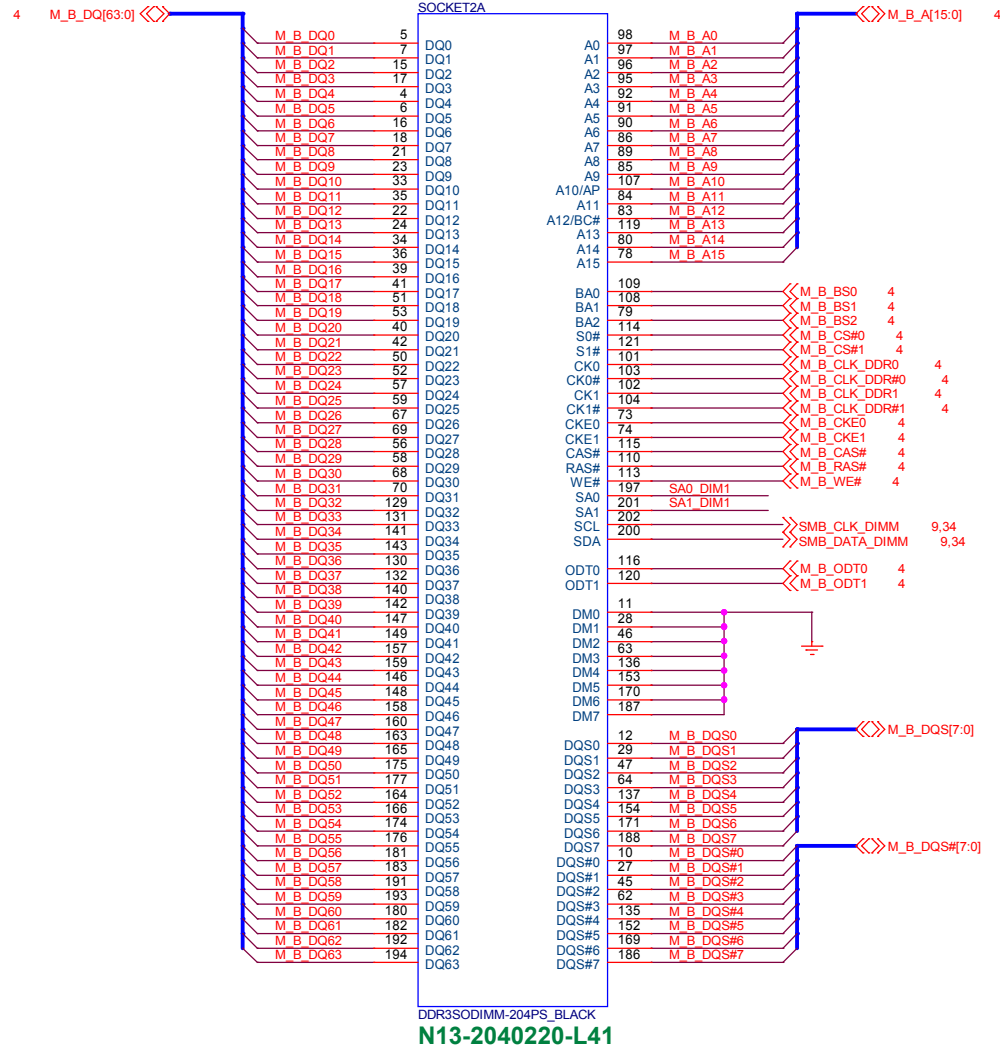
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Title		
CPU-5 (GND)		
Size	Document Number	Rev
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Date:	Thursday, May 29, 2014	Sheet 8 of 72

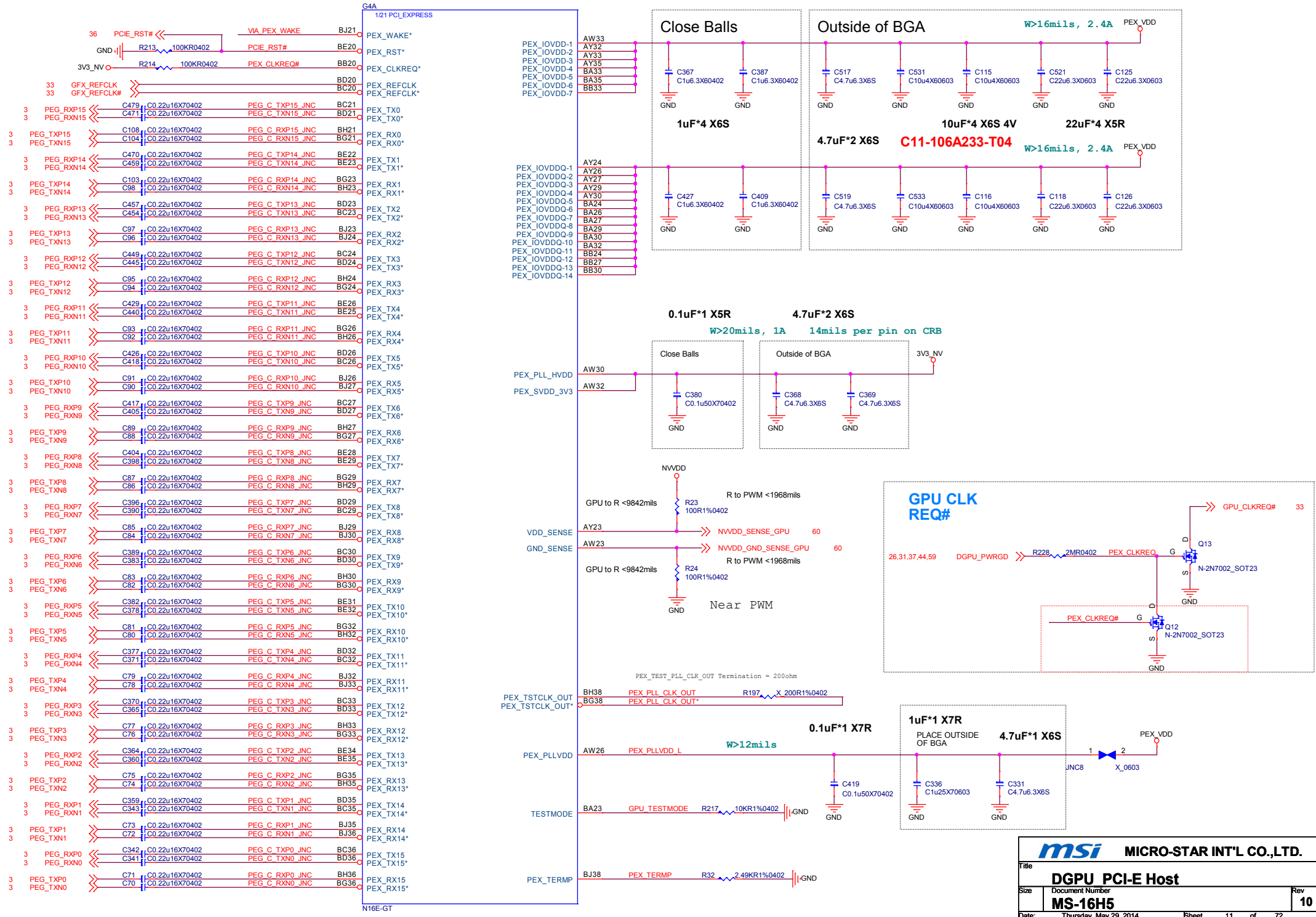
SODIMM#A



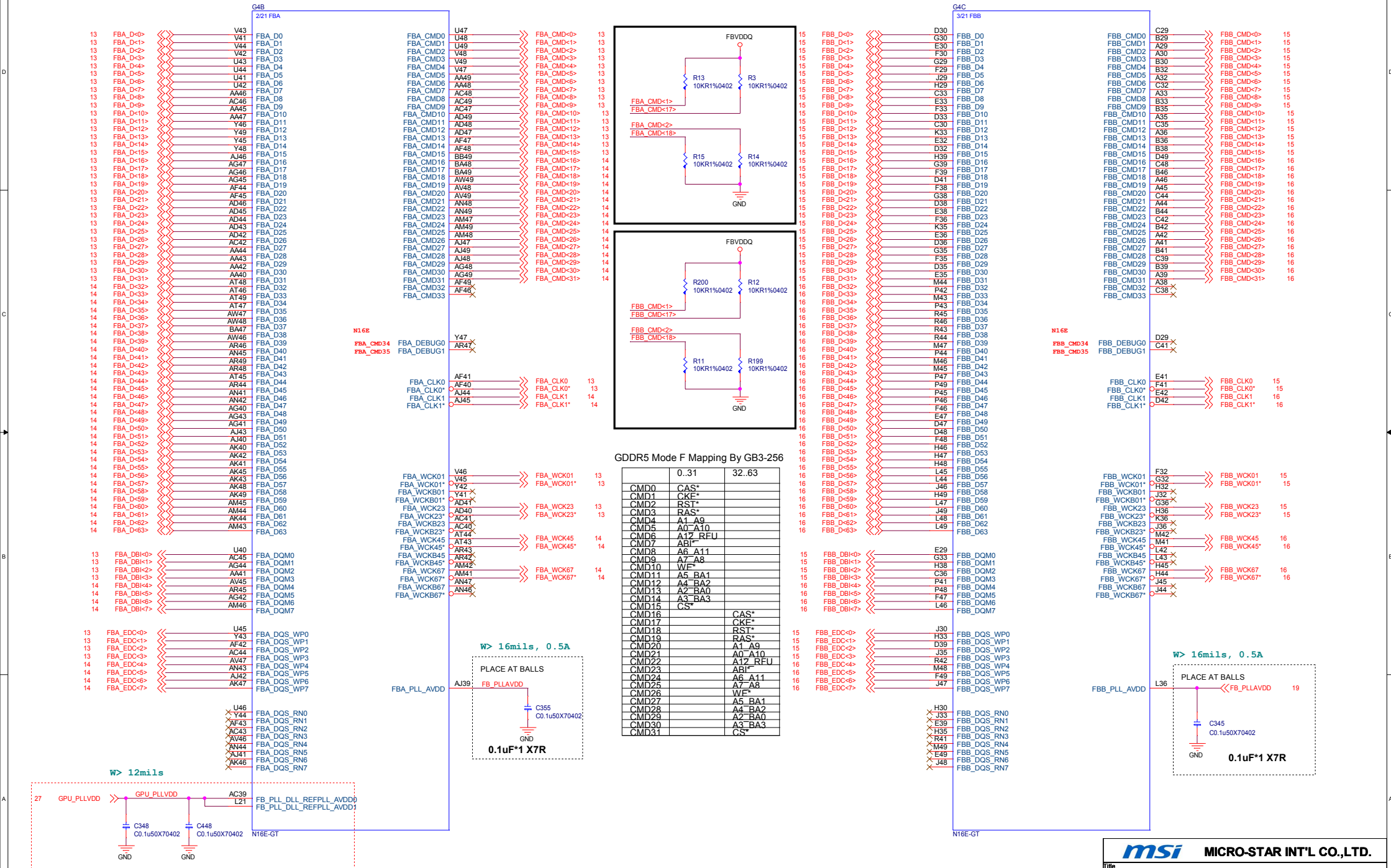
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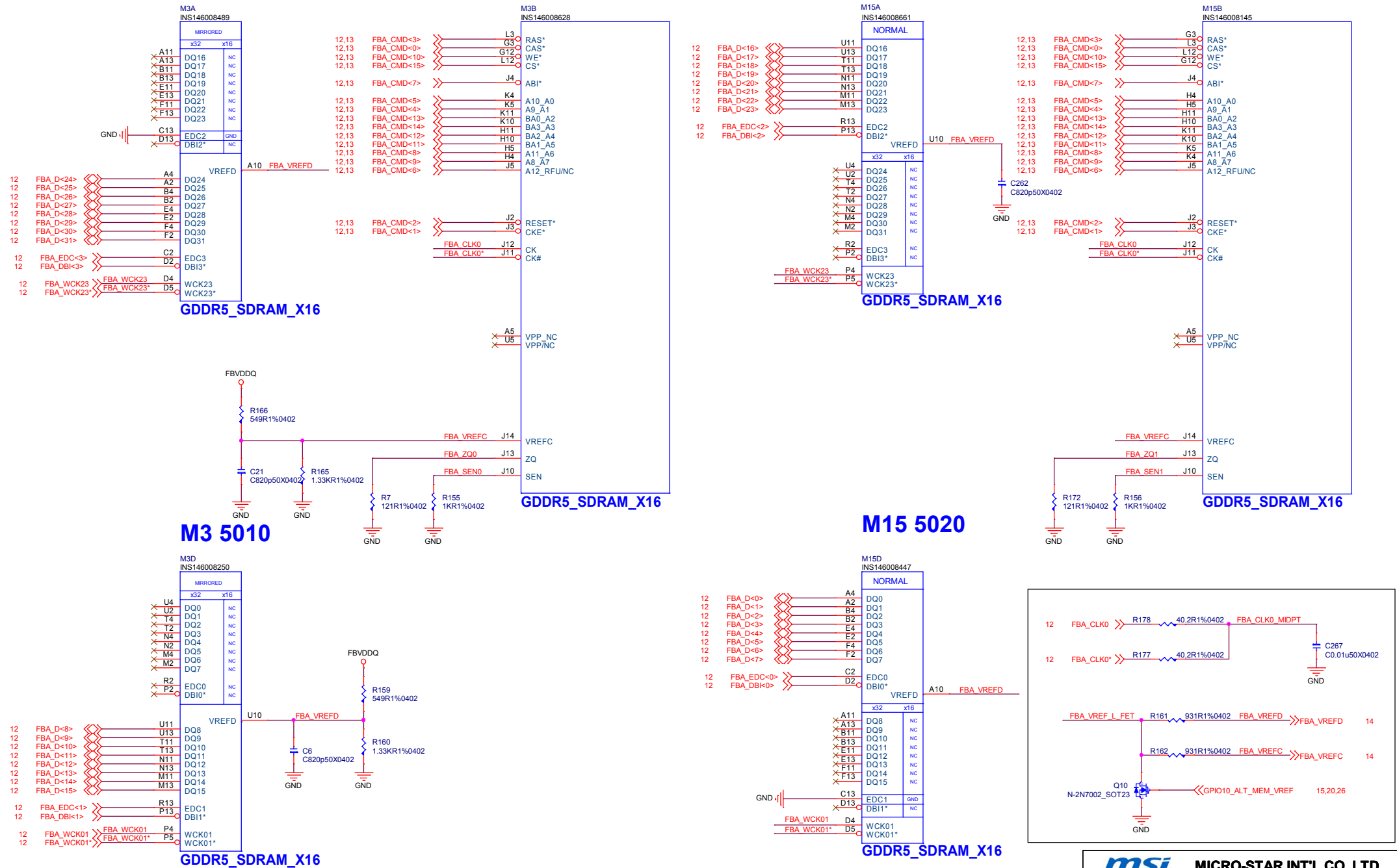
GPU PCI EXPRESS



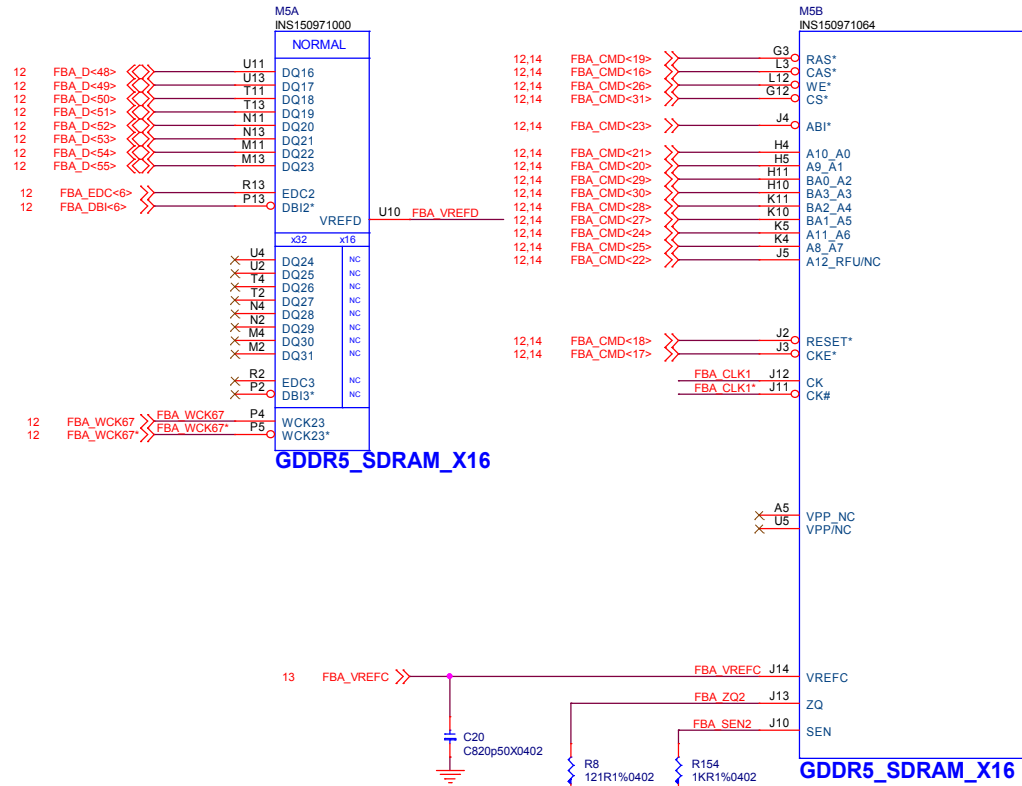
GPU Frame Buffer Partition A/B



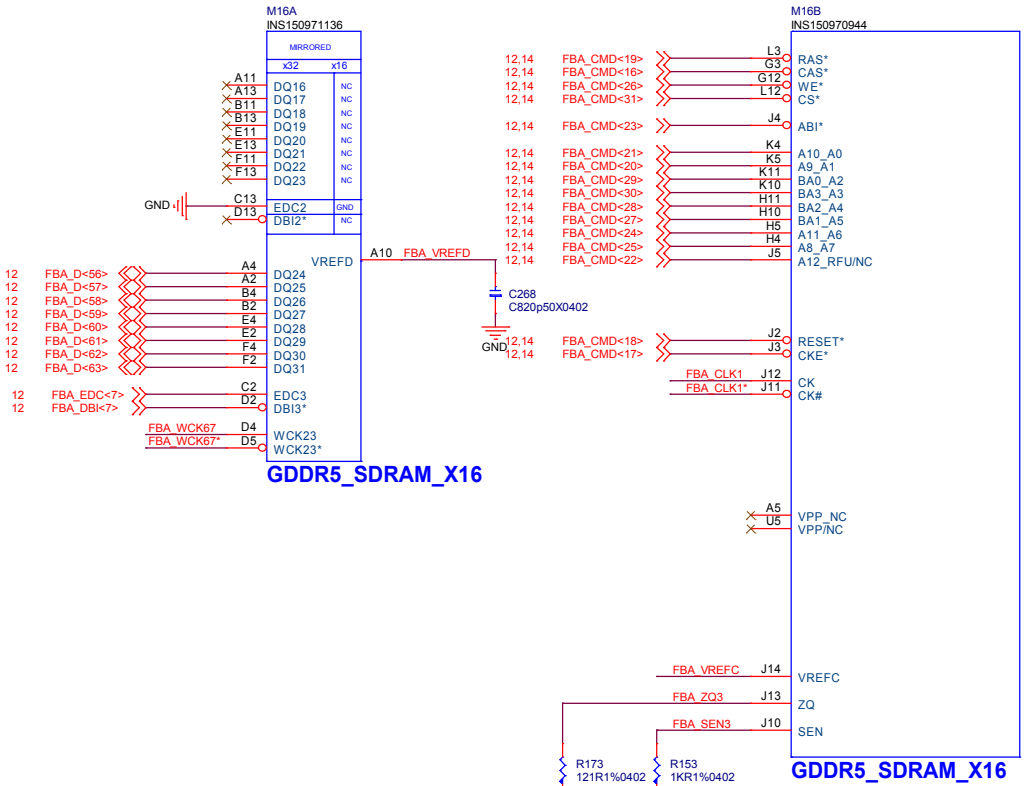
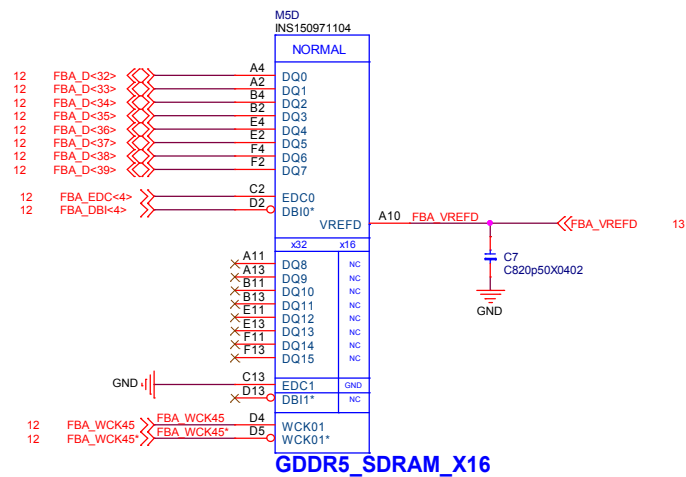
DGPU_GDDR5 FrameBuffer A0



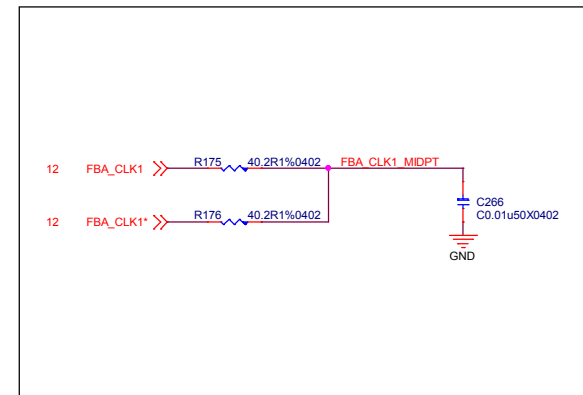
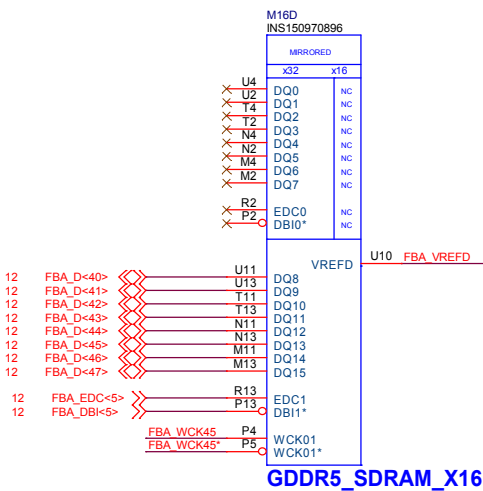
DGPU_GDDR5 FrameBuffer A1



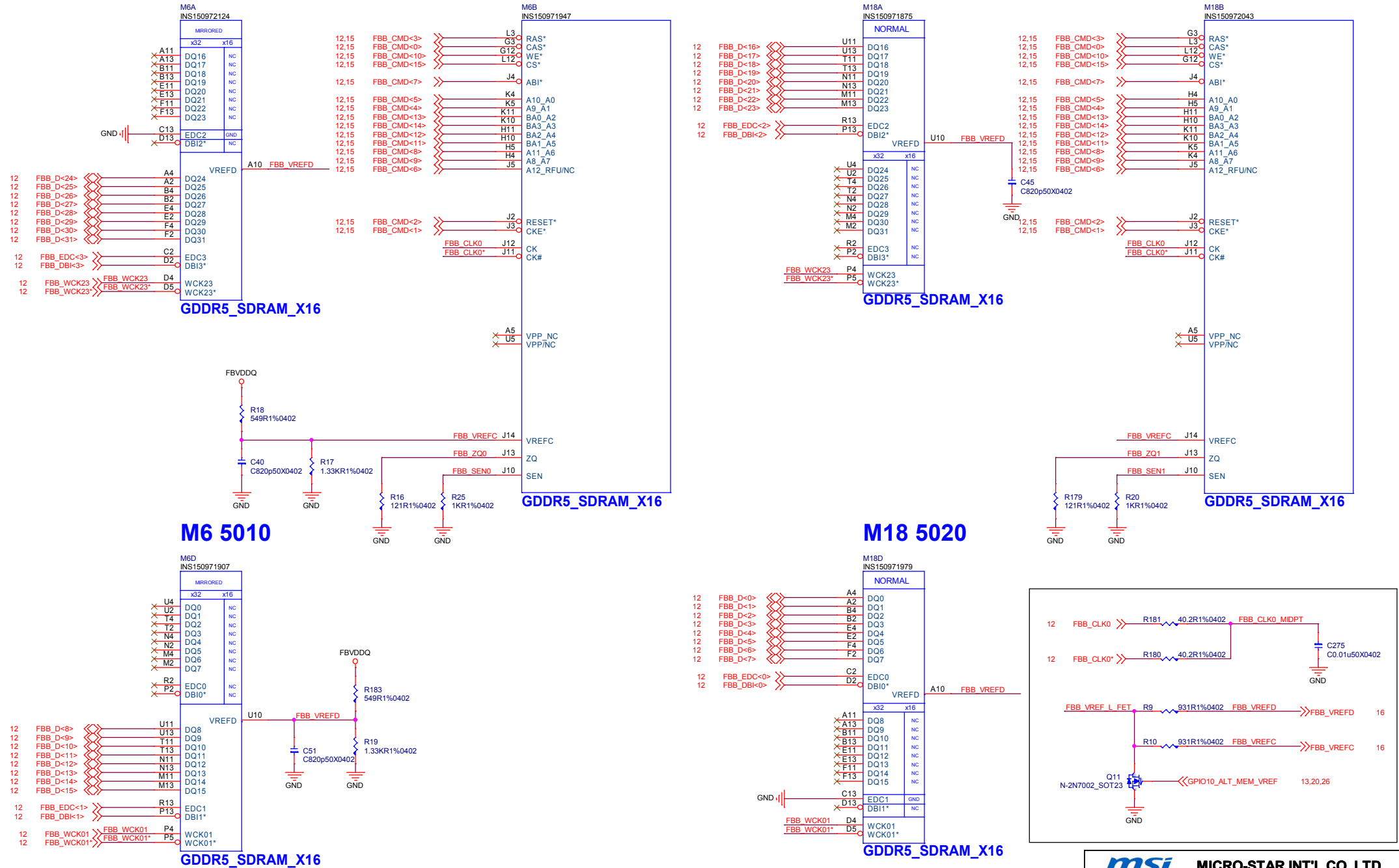
M5 5010



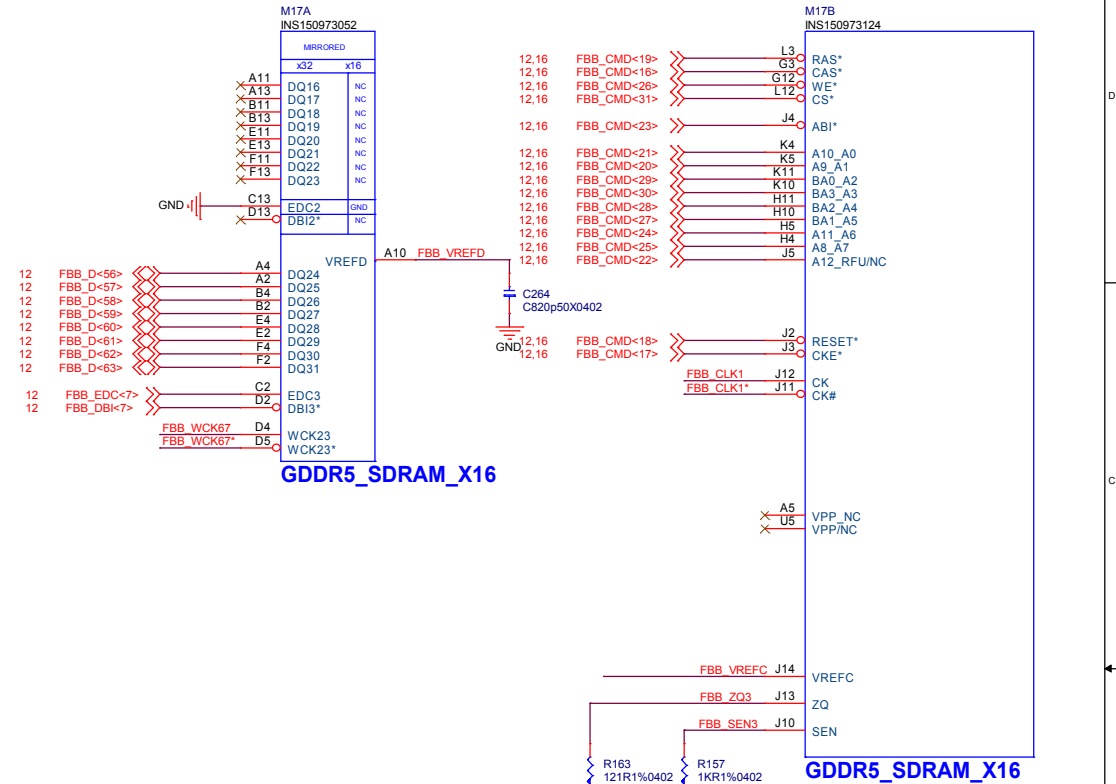
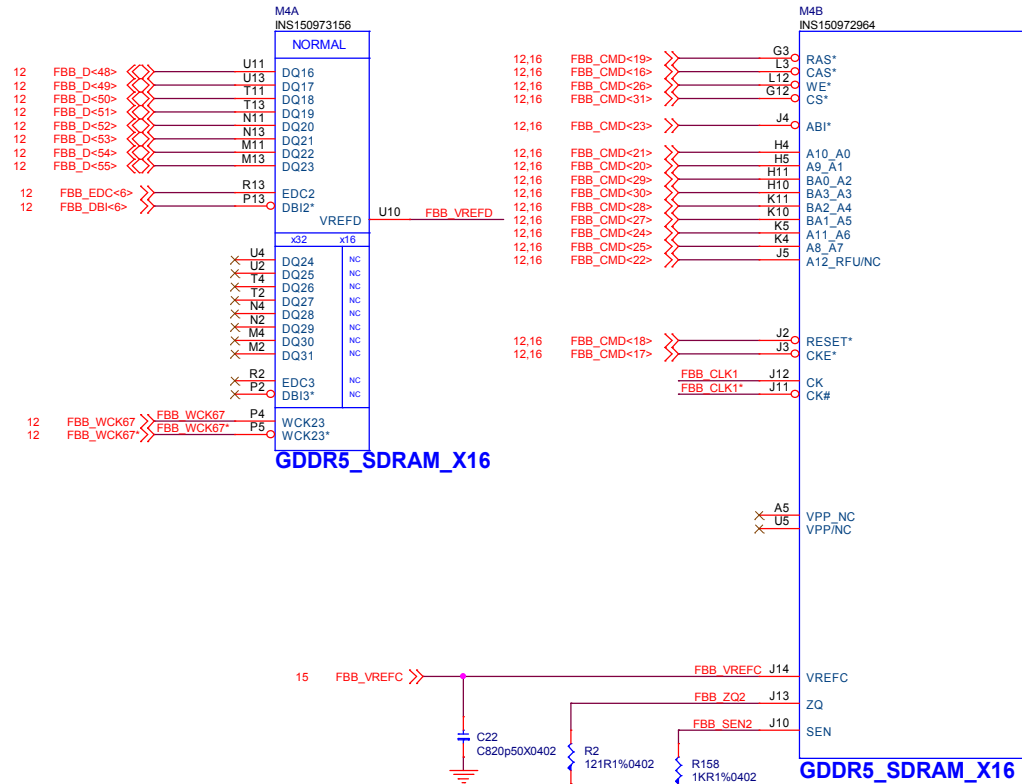
M16 5020



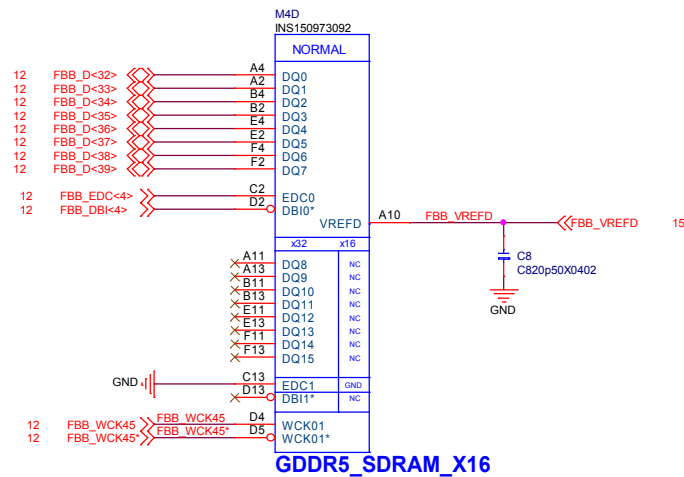
DGPU_GDDR5 FrameBuffer B0



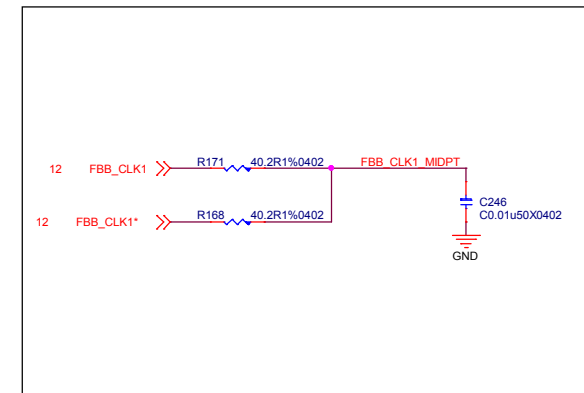
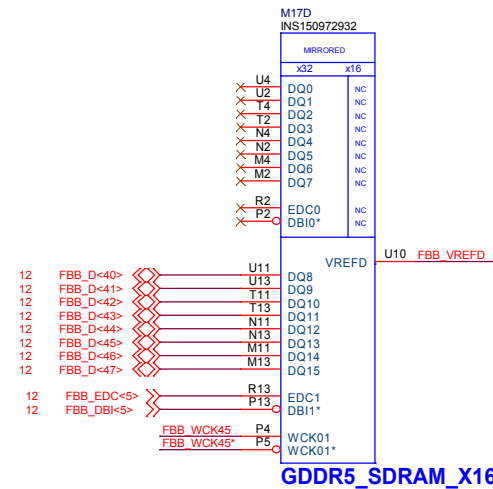
DGPU_GDDR5 FrameBuffer B1



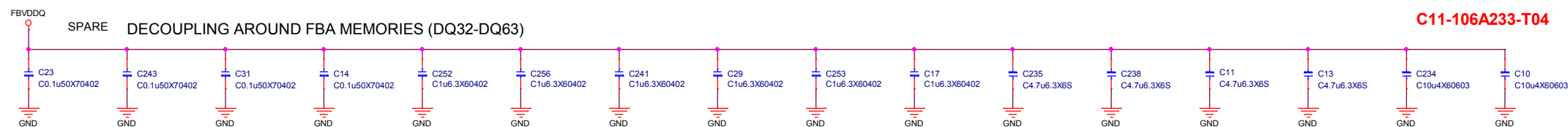
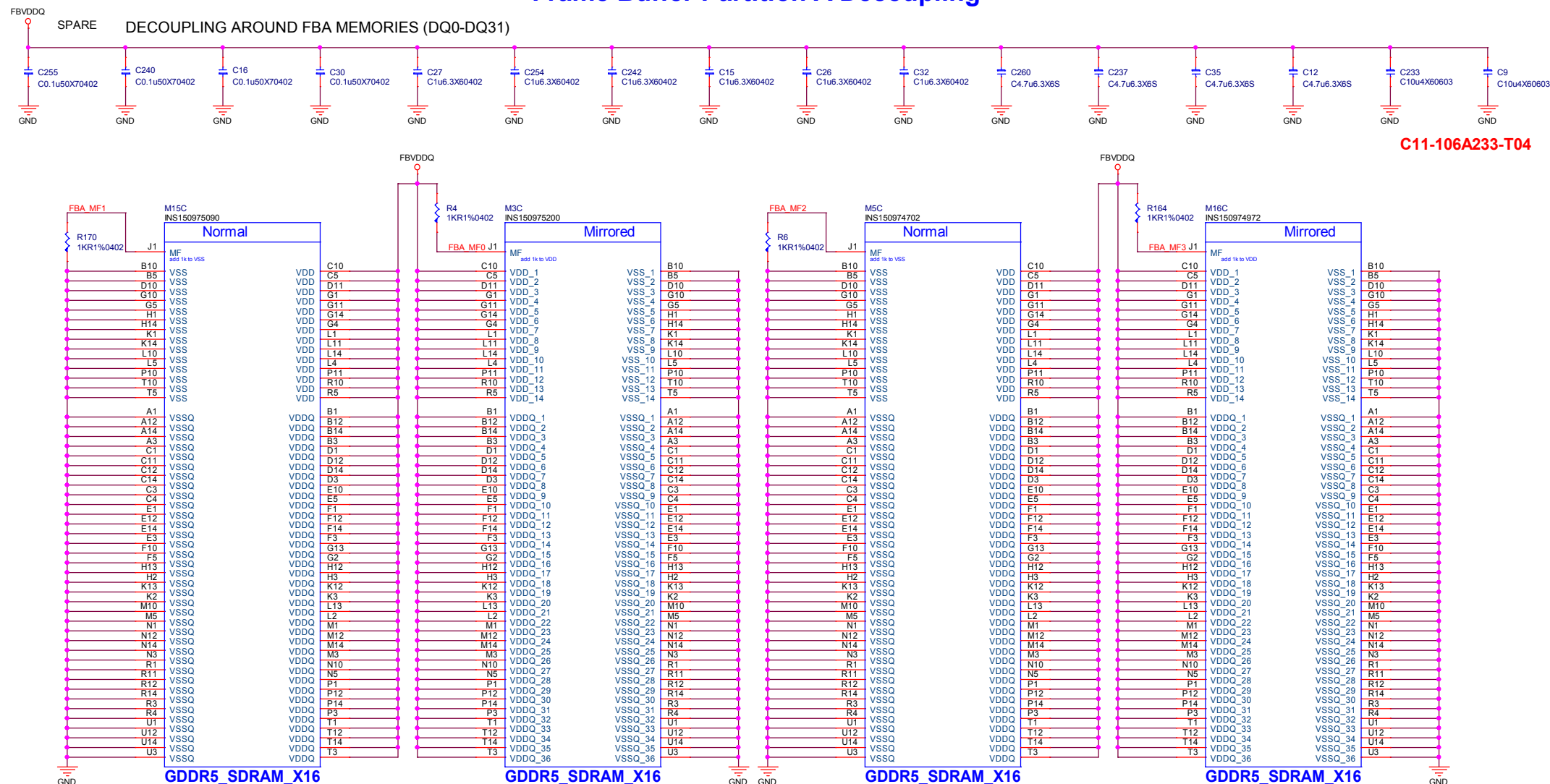
M4 5010



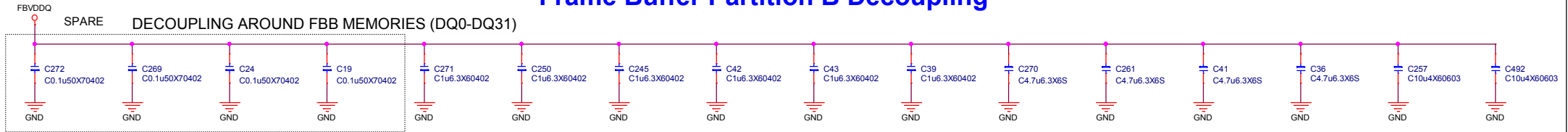
M17 5020



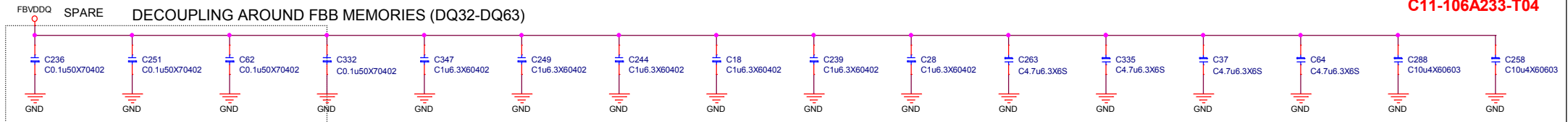
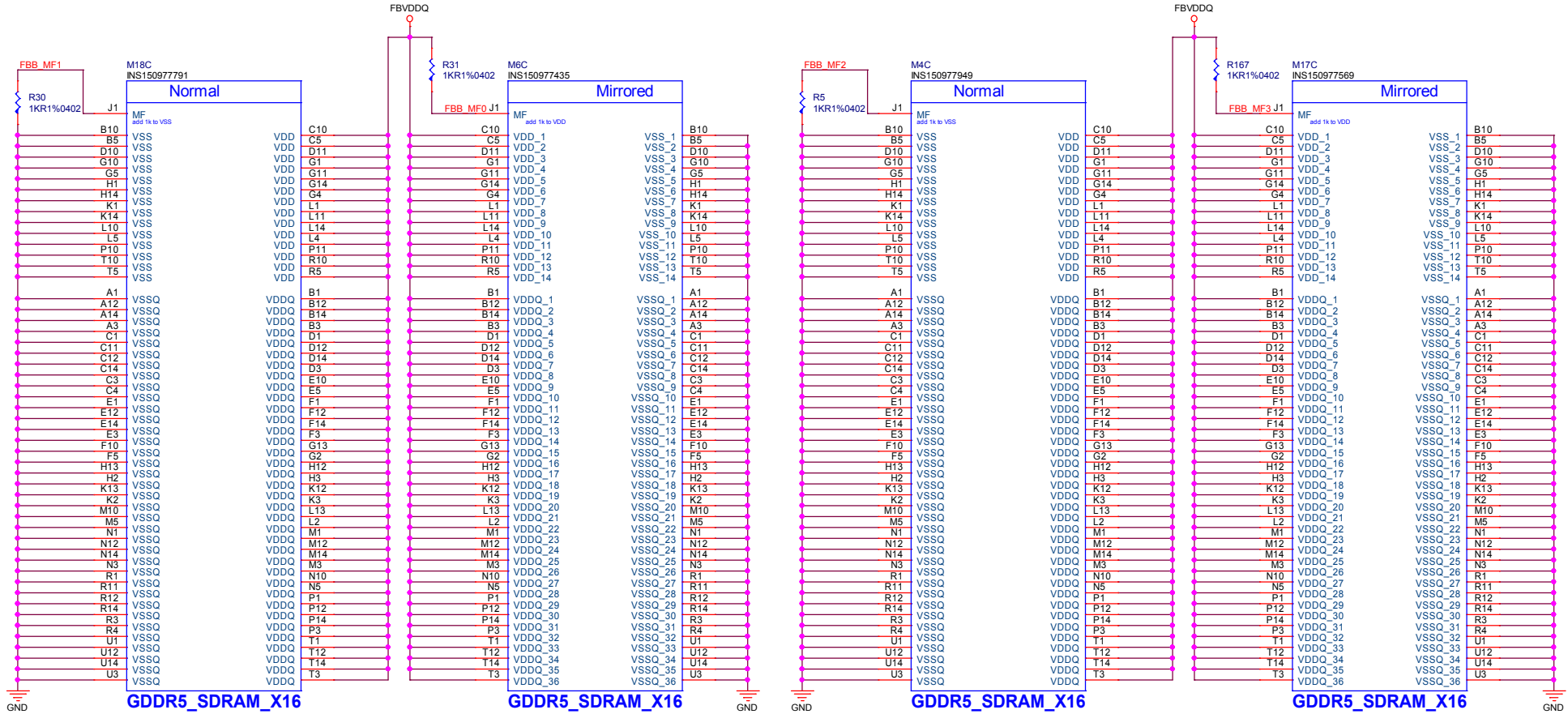
Frame Buffer Partition A Decoupling



Frame Buffer Partition B Decoupling

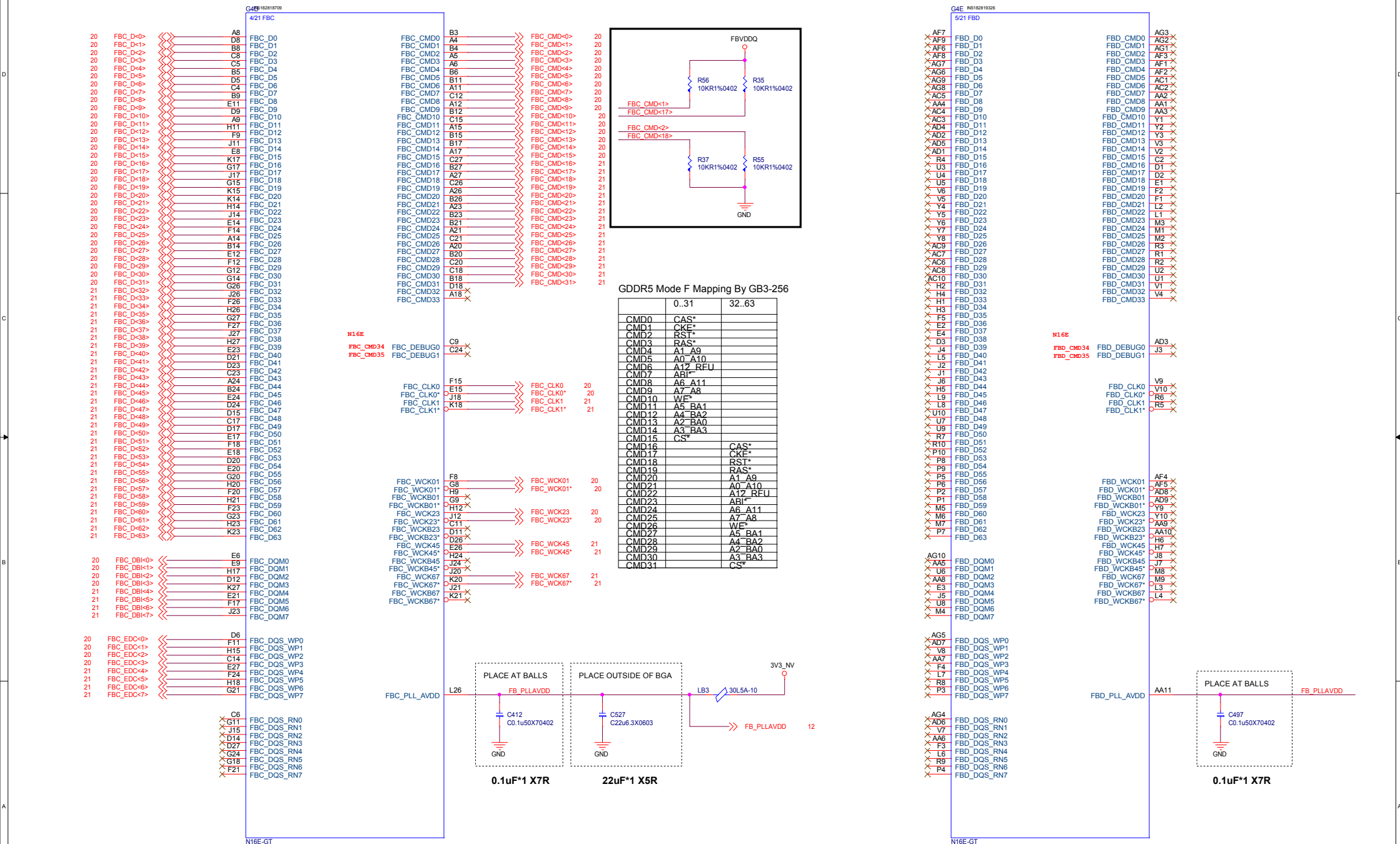


C11-106A233-T04

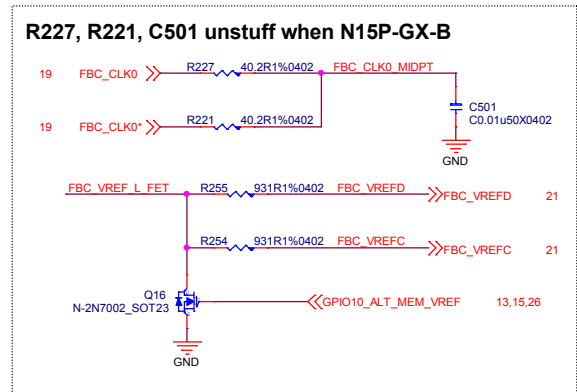
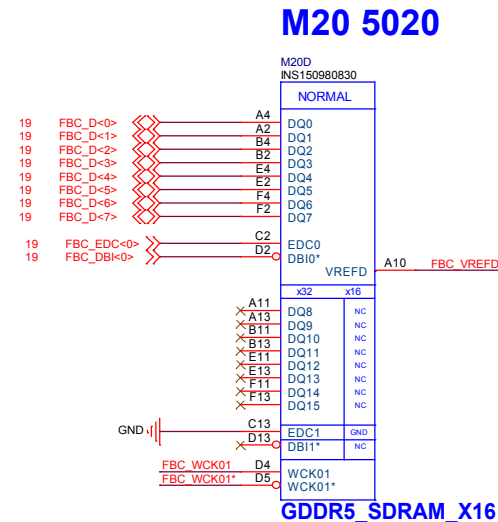
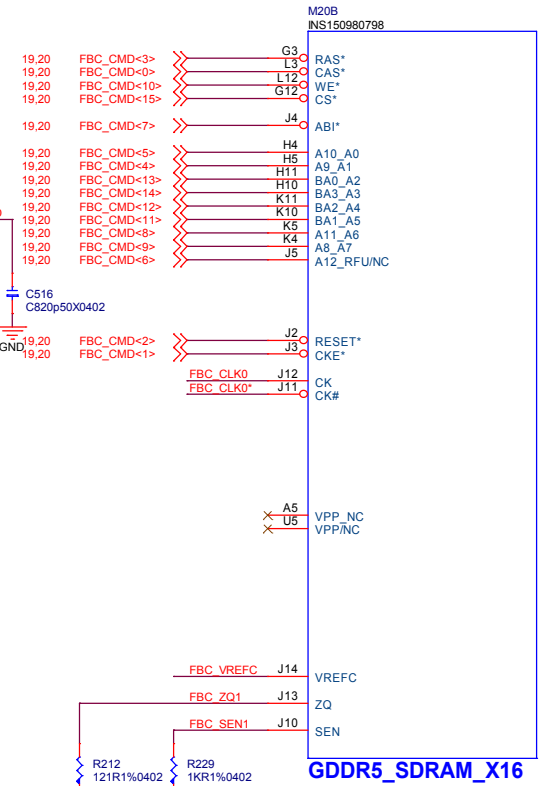


C11-106A233-T04

GPU Frame Buffer Partition C/D

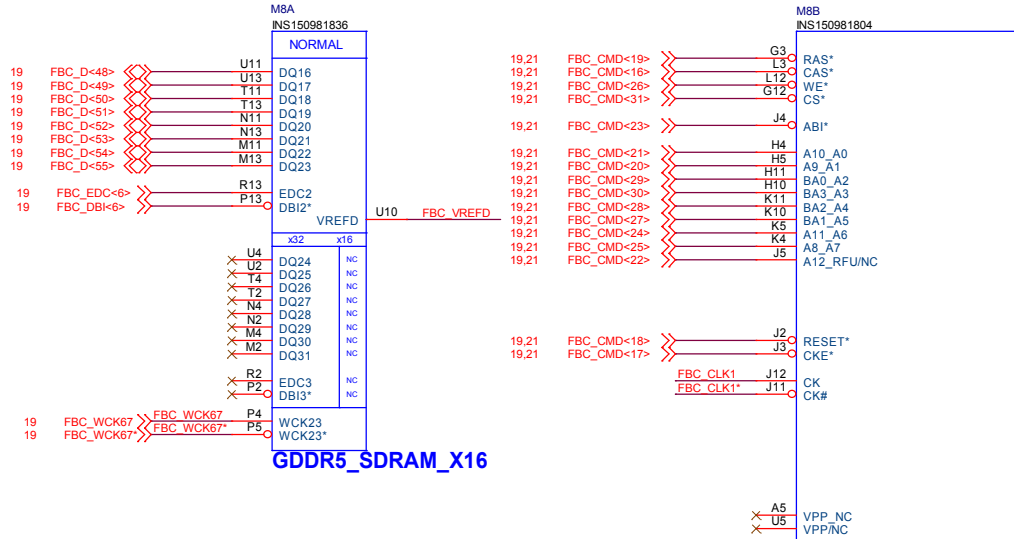


(N16P-GX-B ALL unstuff)

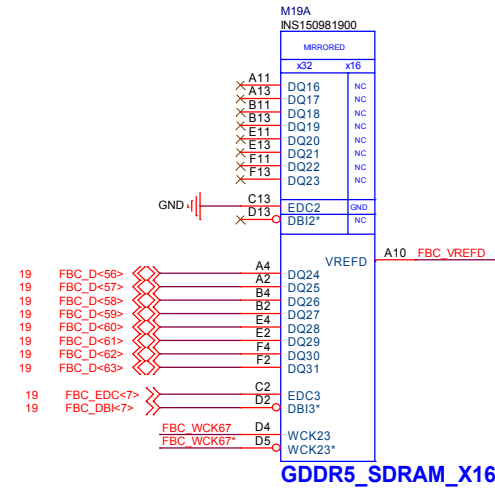


DGPU_GDDR5 FrameBuffer C1

(N16P-GX-B ALL unstuff)

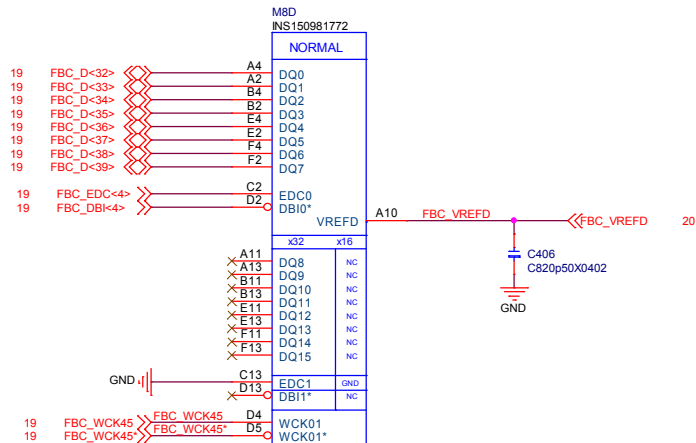


GDDR5_SDRAM_X16



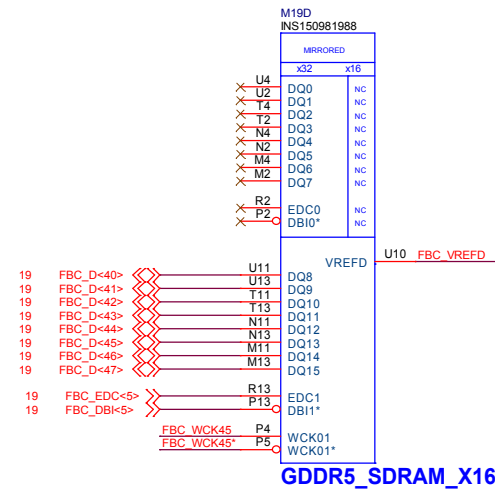
GDDR5_SDRAM_X16

M8 5010



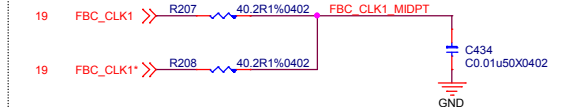
GDDR5_SDRAM_X16

M19 5020



GDDR5_SDRAM_X16

R227, R221, C501 unstuff when N15P-GX-B



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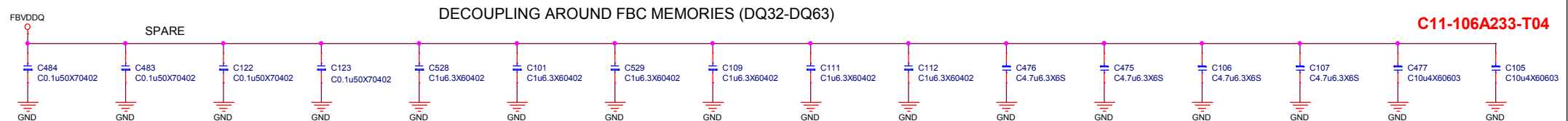
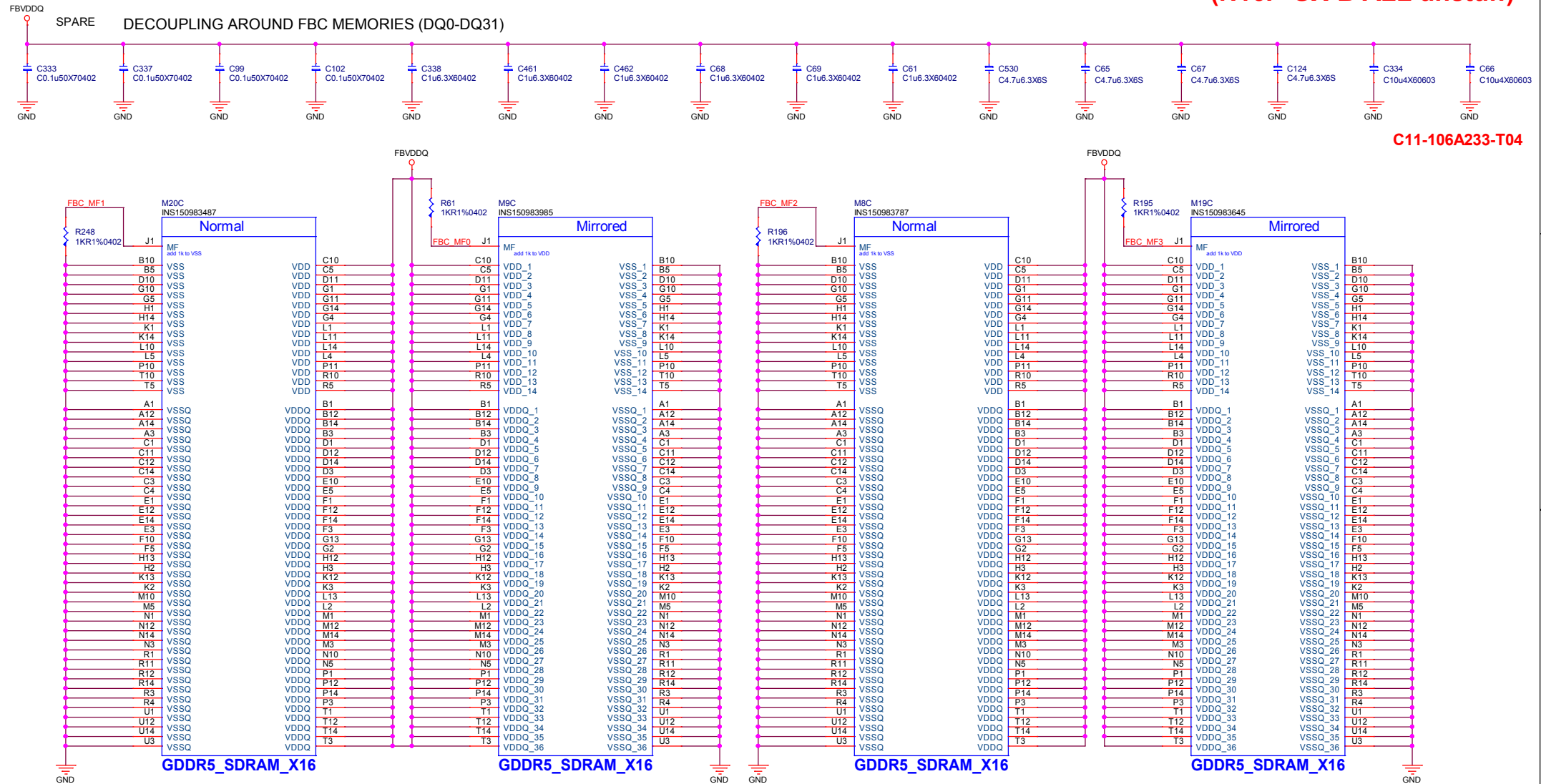
DGPU_GDDR5 FrameBuffer C

Size Document Number **MS-16H5** Rev **10**

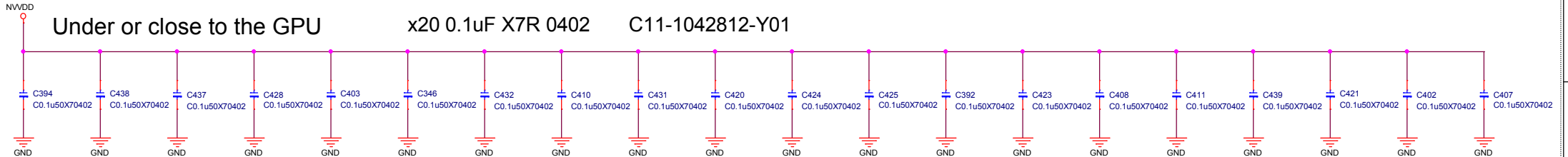
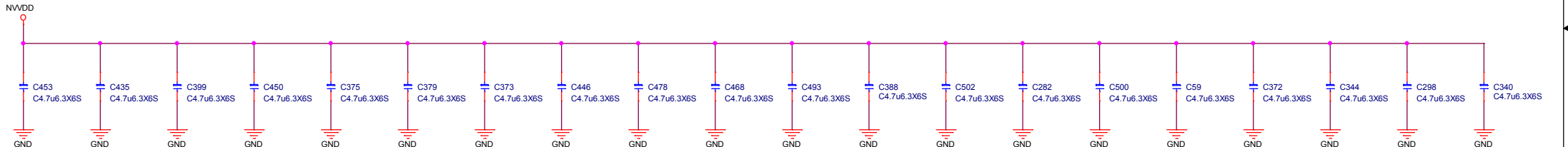
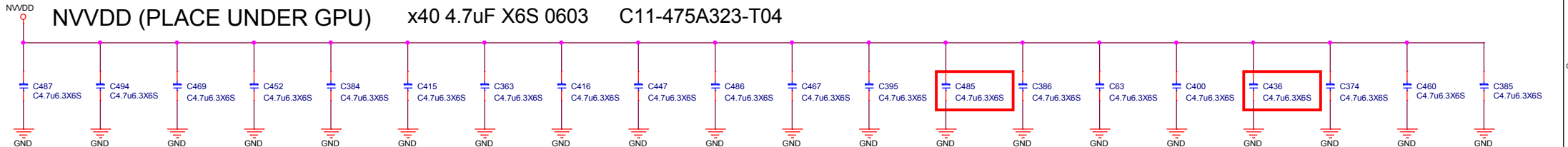
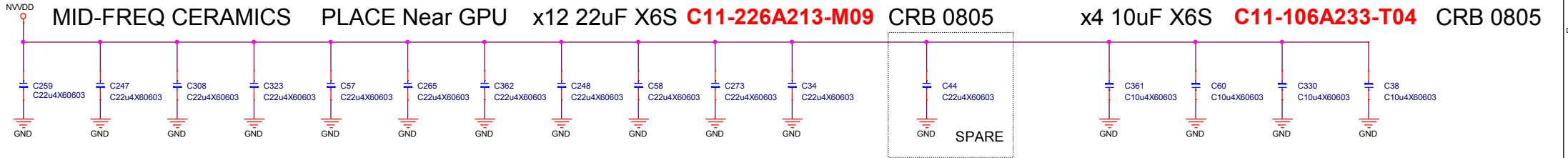
Date: Thursday, May 29, 2014 Sheet 21 of 72

Frame Buffer Partition C Decoupling

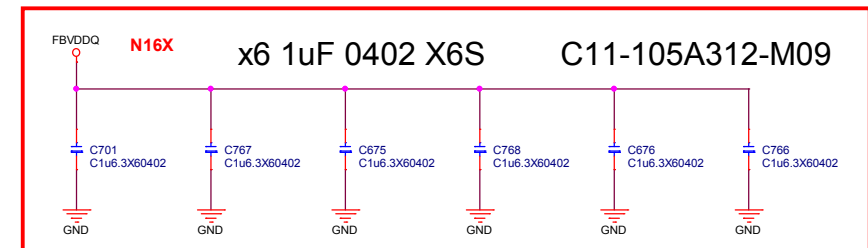
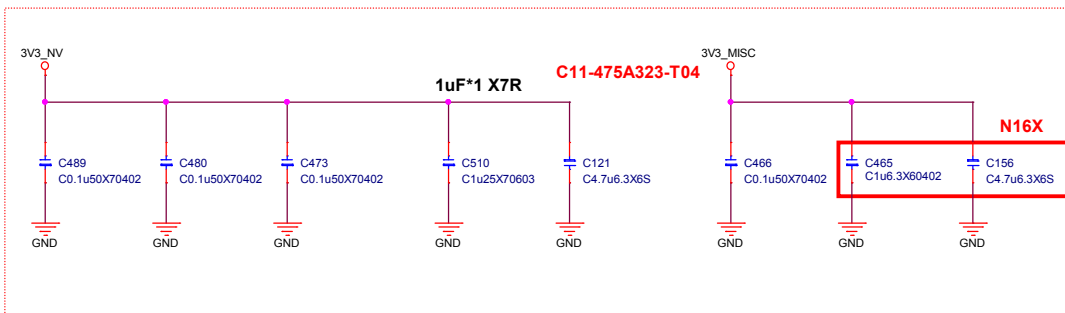
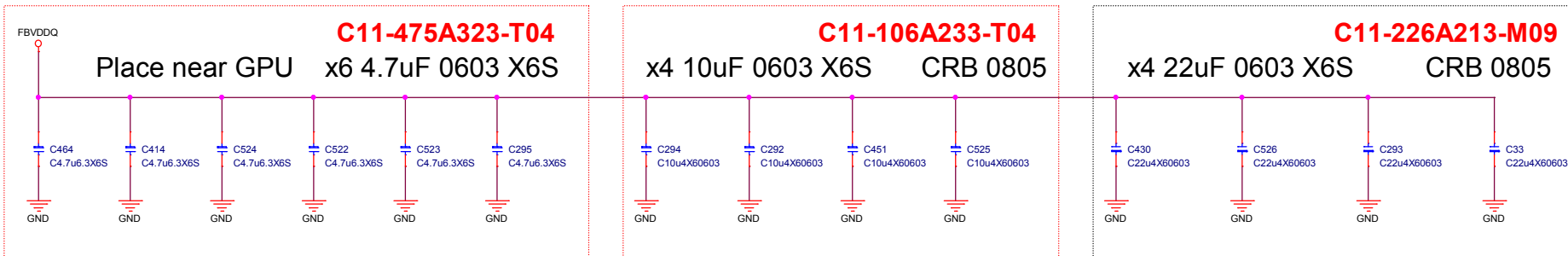
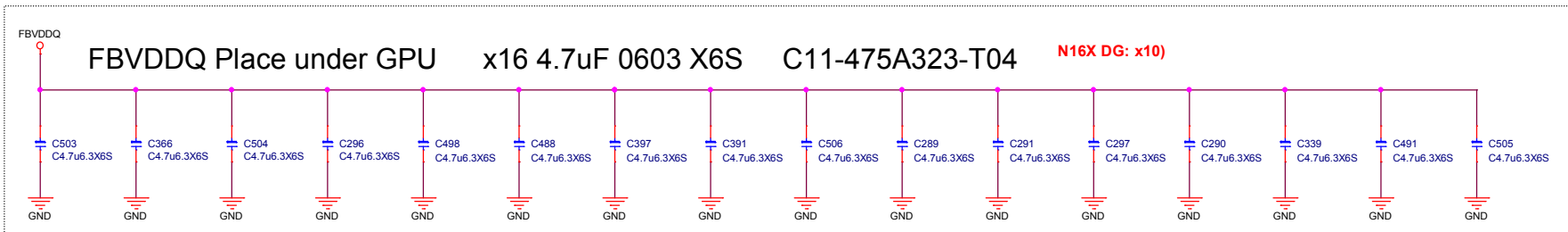
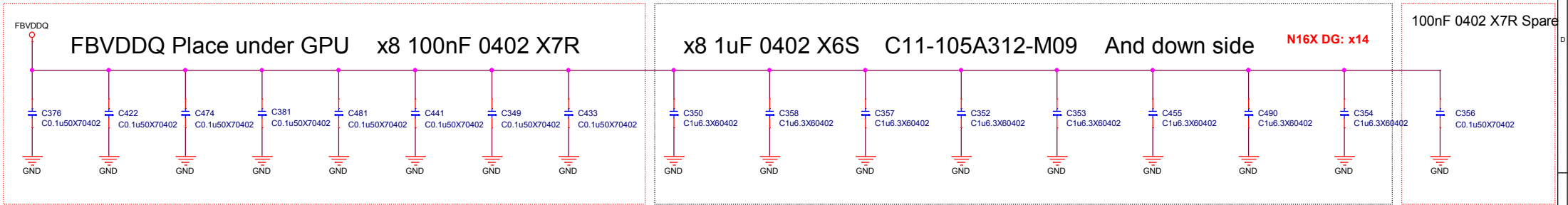
(N16P-GX-B ALL unstuff)



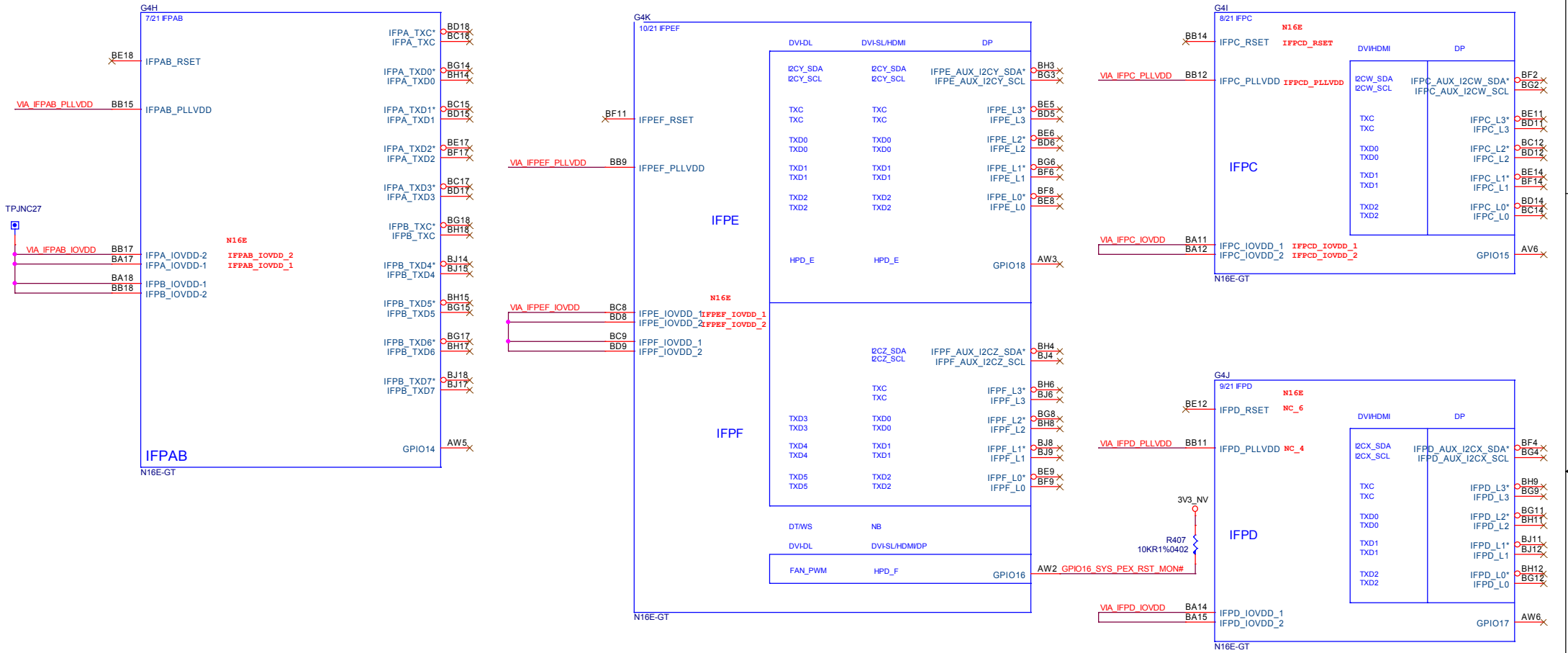
GPU DECOUPLING A



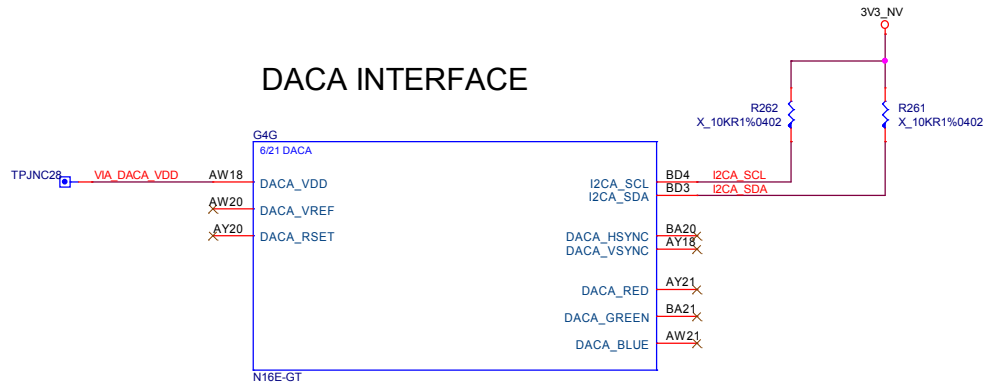
GPU DECOUPLING B



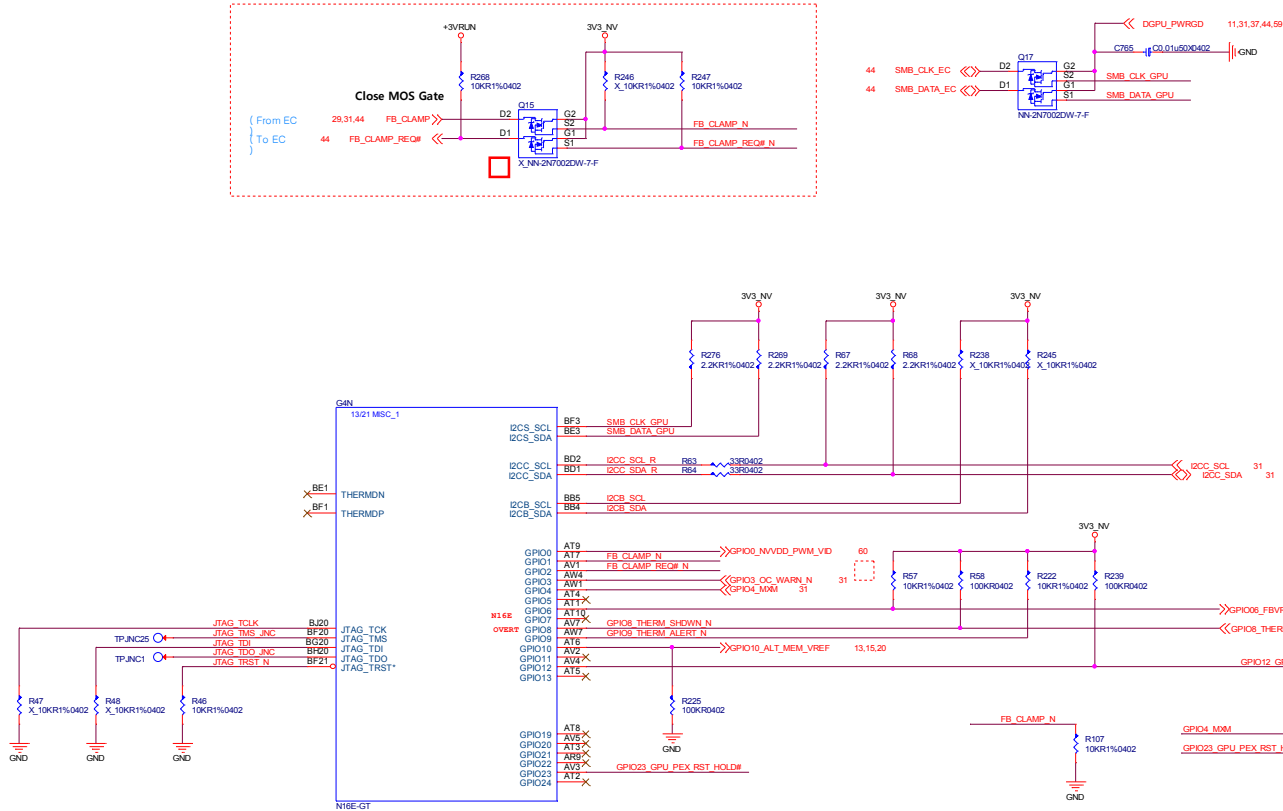
DACA,Display IF



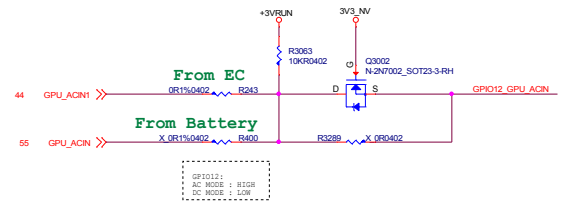
DACA INTERFACE



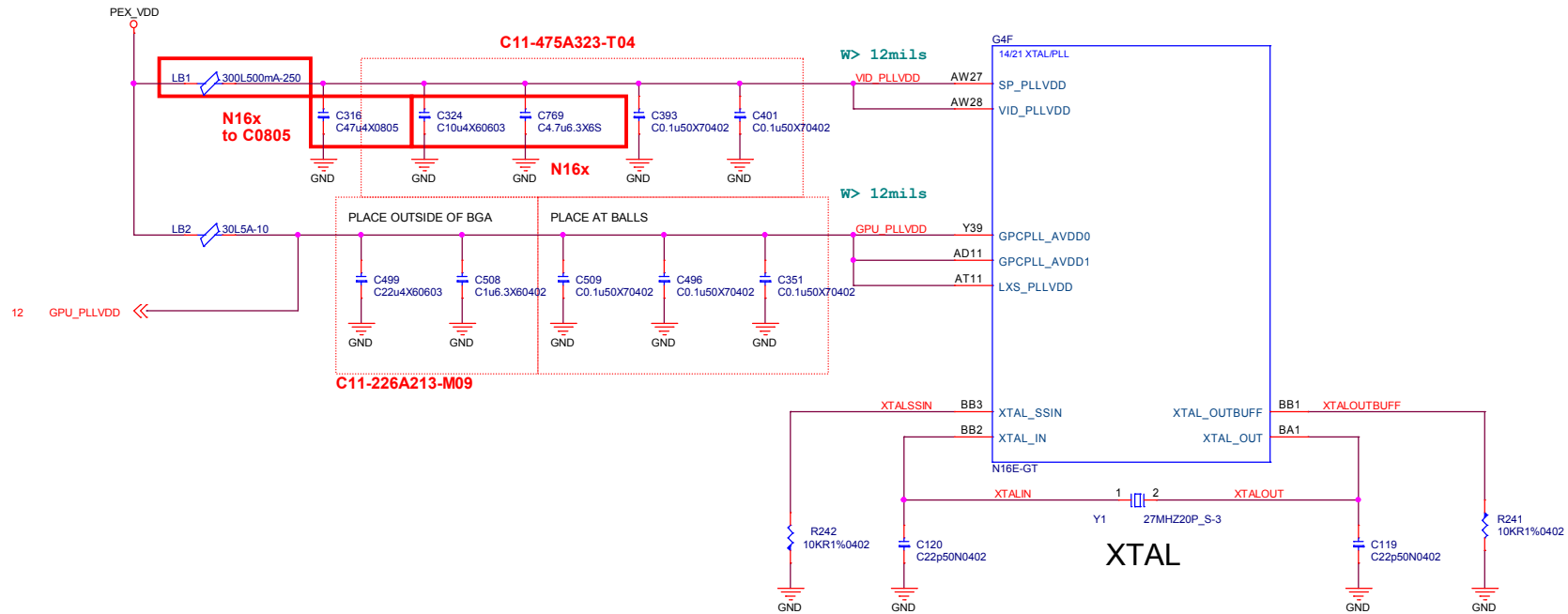
DGPU GPIO, I2C



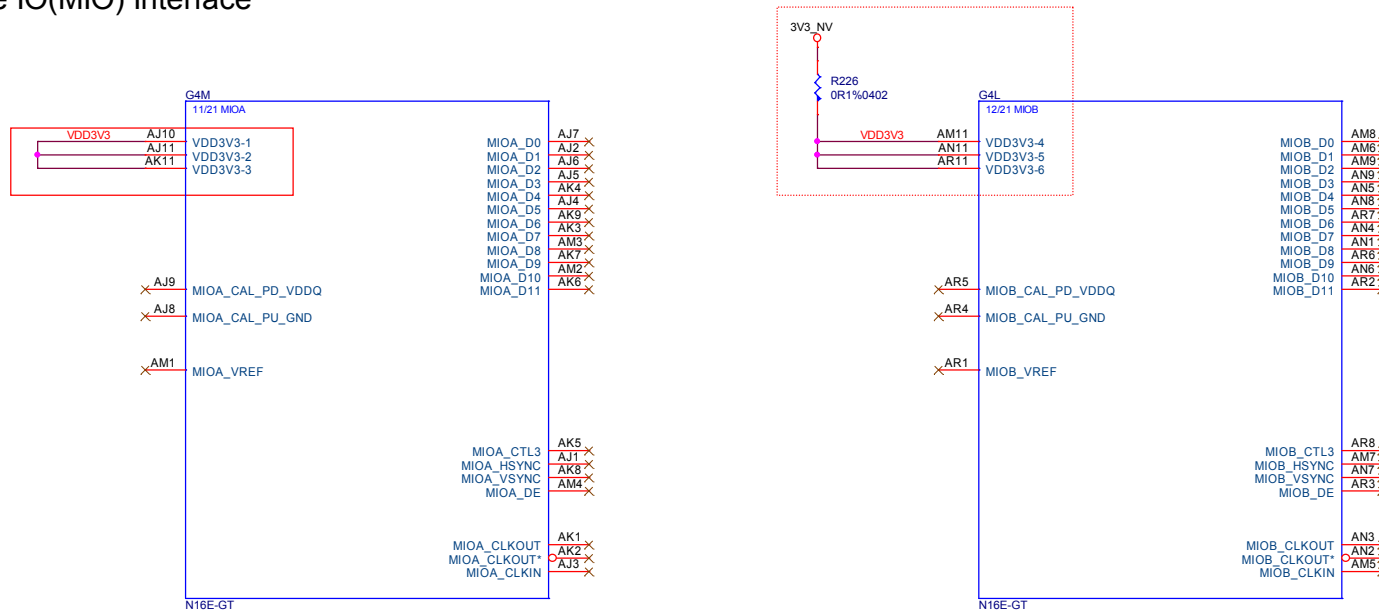
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO3	OC_WARN	I	Over current throttling	10K pull-up to 3V3_AON
GPIO4	3V3_MAIN_EN	O	GPU POWER Sequencing for GC6 2.0	10K pull-up to 3V3_AON
GPIO5	RESERVED			
GPIO6	PSI	O	Phase shedding	
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPAB	
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3_AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	RESERVED			
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	1K pull-up to 3V3_AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
GPIO24	MEM_VDD_CTL	O	Memory VDD VID	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_B	I	Hot Plug Detect for IFPB	
OVERT	OVERT(OVERT#)	I/O	Catastrophic Over Temperature	100K pull-up to 3V3_AON



DGPU MIO & XTAL



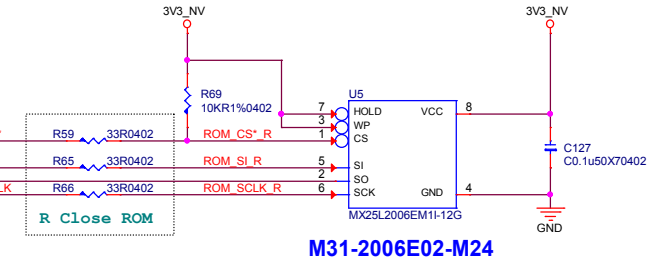
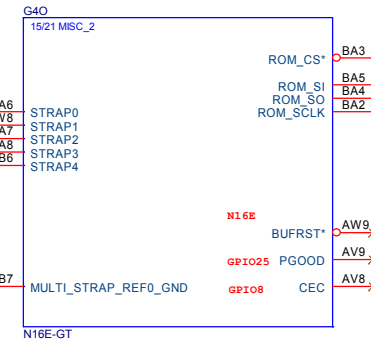
Multi-use IO(MIO) Interface



ROM, MULTI-LEVEL STRAPS

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

STRAP0 BA6
STRAP1 AW8
STRAP2 BA7
STRAP3 BA8
STRAP4 BB6



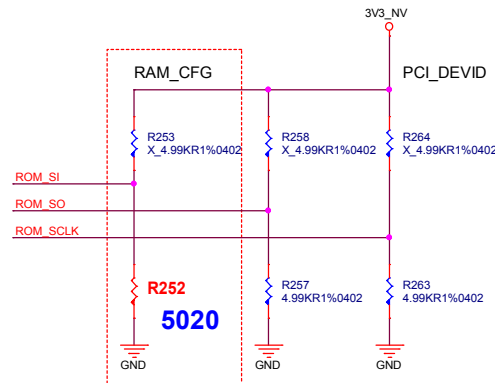
M31-2006E02-M24

ROM_SI35K	Hynix	V_TOP1	V_BOT1
128Mx16bit	5010	5020	
R11-3482T12-W08	M12-5GC2H05-H23	M12-5GC2H05-H23	
X_34.8KR1%0402	X_H5GC2H24BFR-T2C	X_H5GC2H24BFR-T2C	

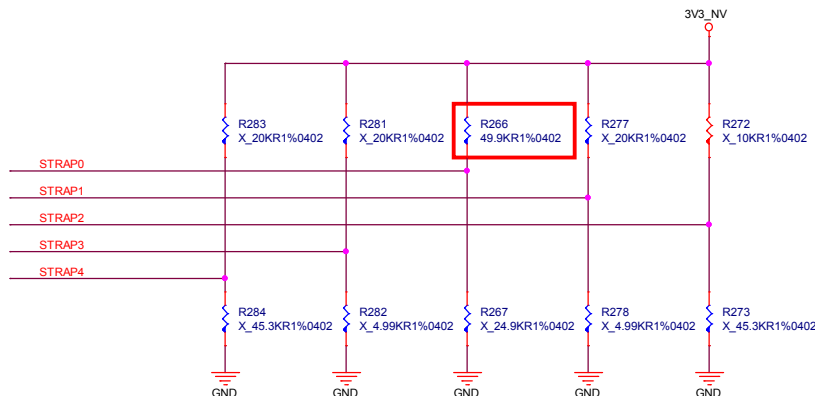
ROM_SI45K	Samsung	V_TOP2	V_BOT2
128Mx16bit	5010	5020	
R11-4532T12-W08	M12-2032585-S02	M12-2032585-S02	
X_45.3KR1%0402	X_K4G20325FD-FC03	X_K4G20325FD-FC03	

GDDR5 Parts

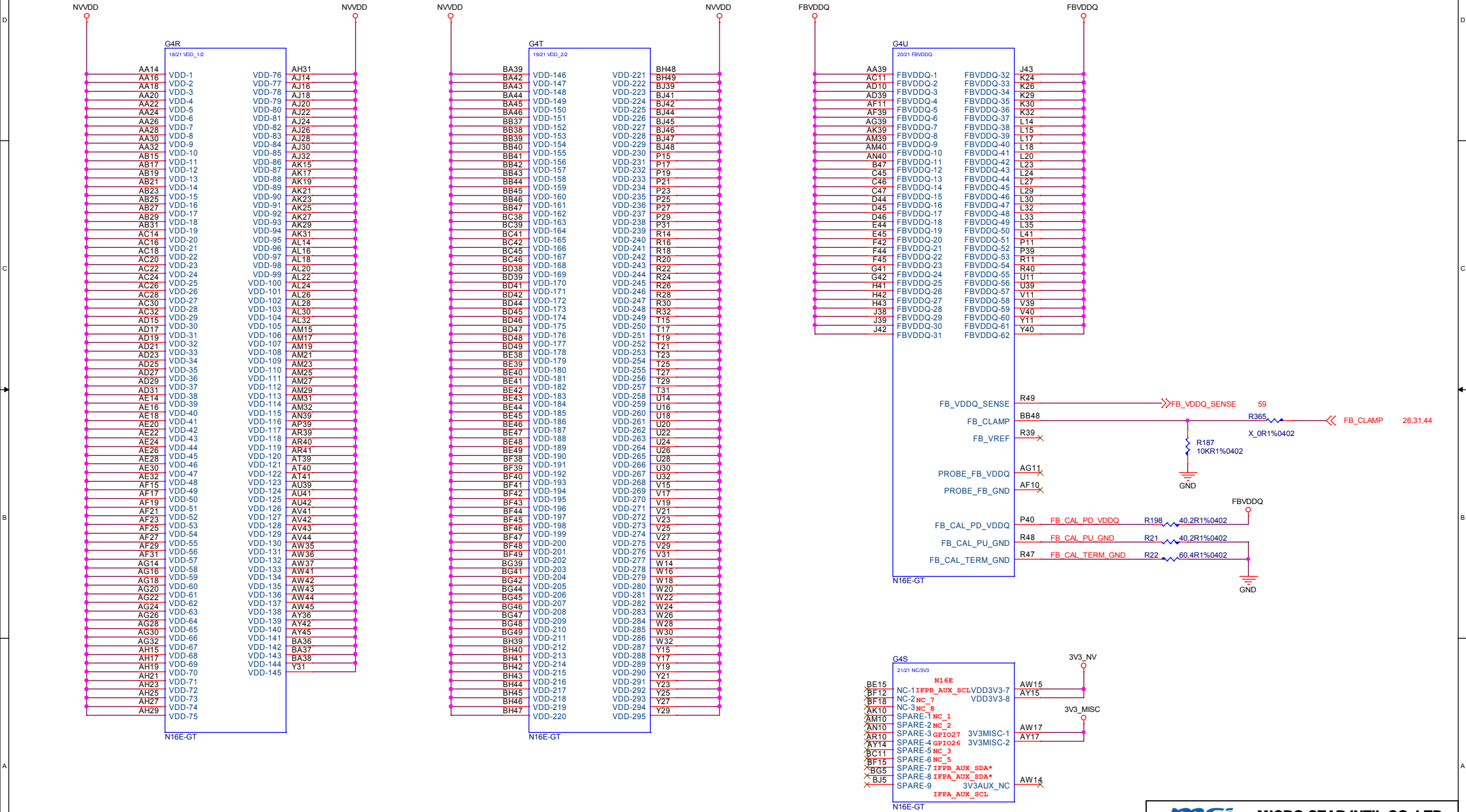
5010 : M4 , M3 , M5 , M6 , M8 , M9
5020 : M17, M15, M16, M18, M19, M20



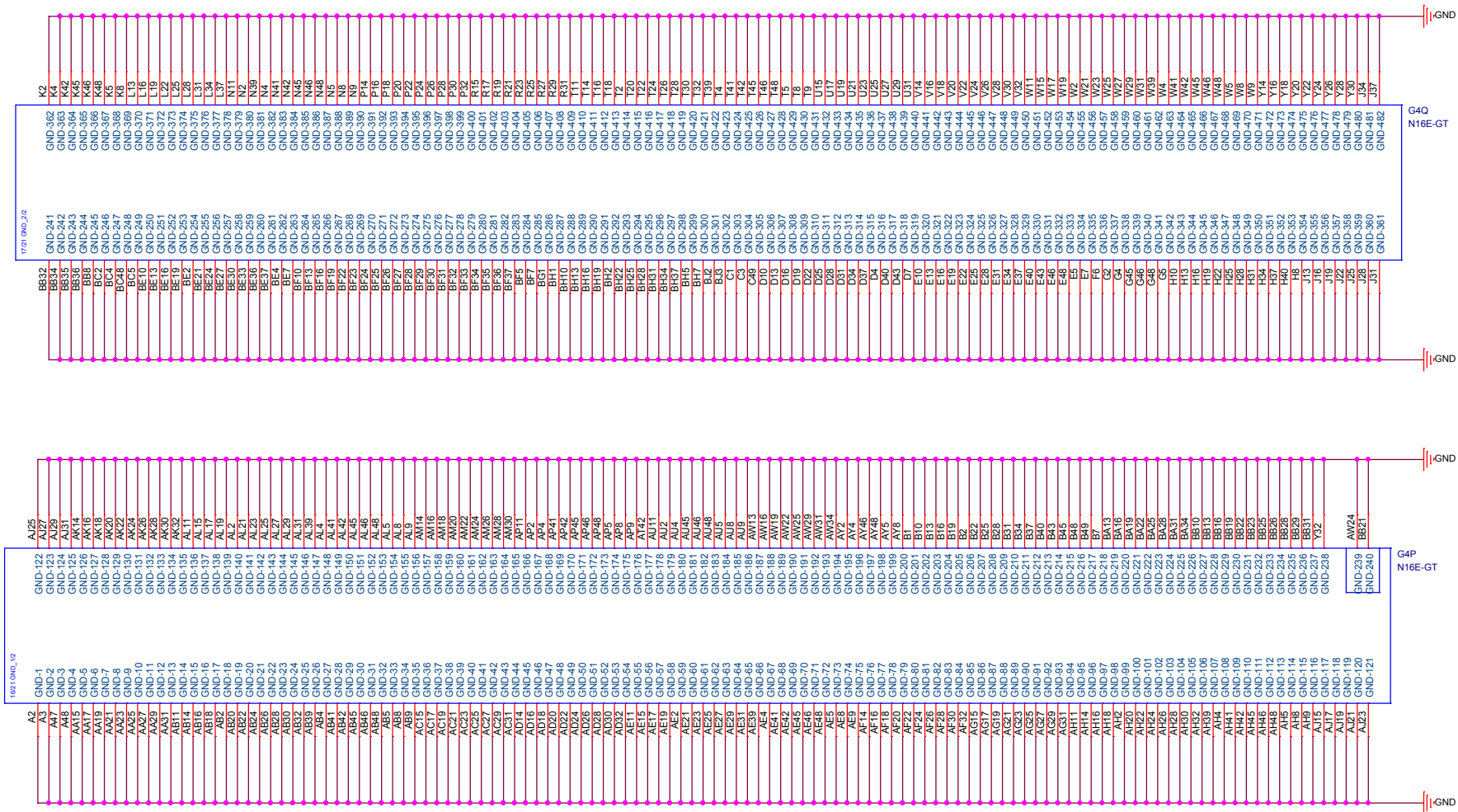
ROM_SI	35K PD	Hynix 128x16bit
	45K PD	Samsung 128x16bit
ROM_SO	5K PD	
ROM_SCLK	5K PD	
STRAP0	50K PU 3V3_AON	
STRAP1	Reserved	
STRAP2	Reserved	
STRAP3	Reserved	
STRAP4	Reserved	



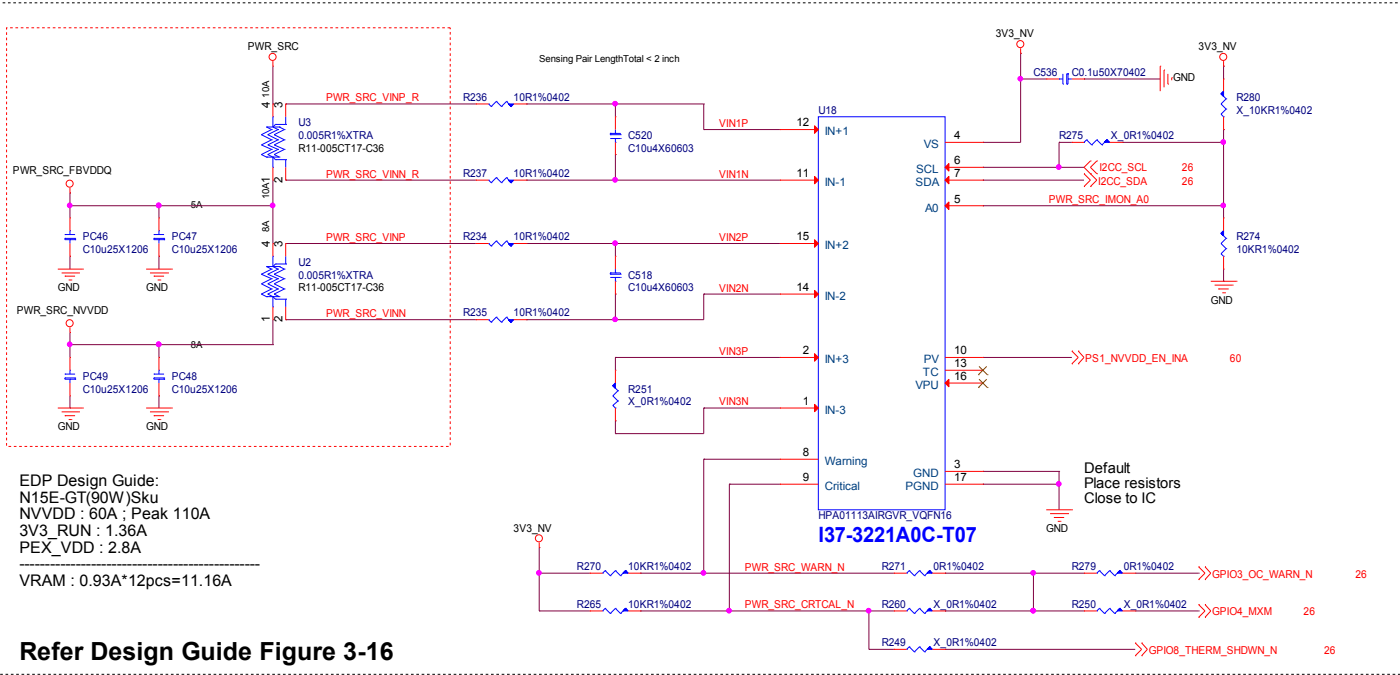
GPU NVVDD, FBVDDQ



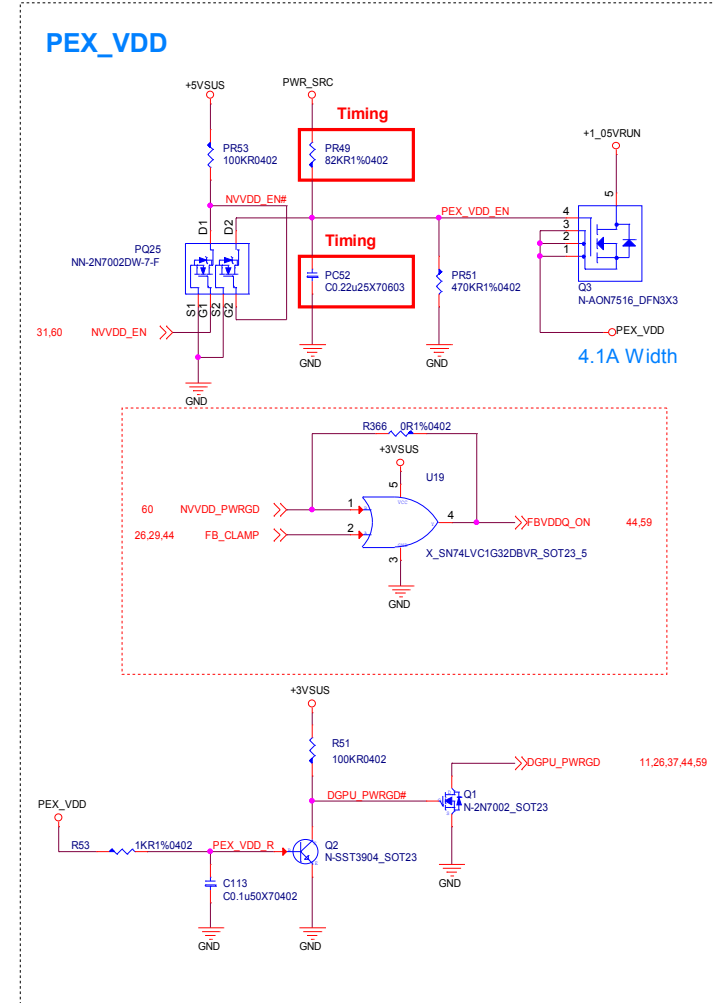
DGPU GND



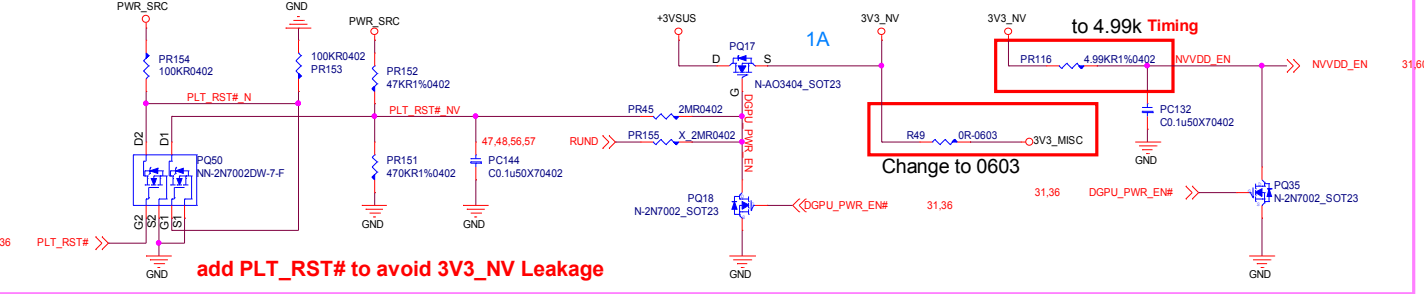
DGPU_Power Control



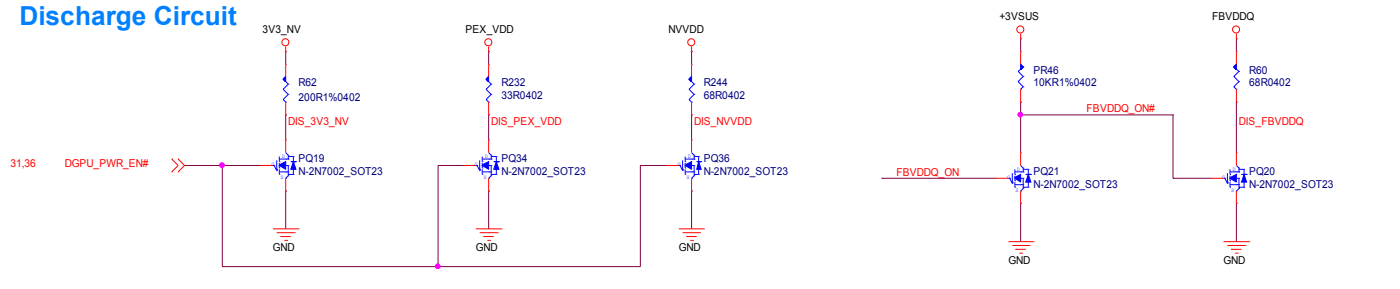
Refer Design Guide Figure 3-16



nVIDIA Power Sequence Control

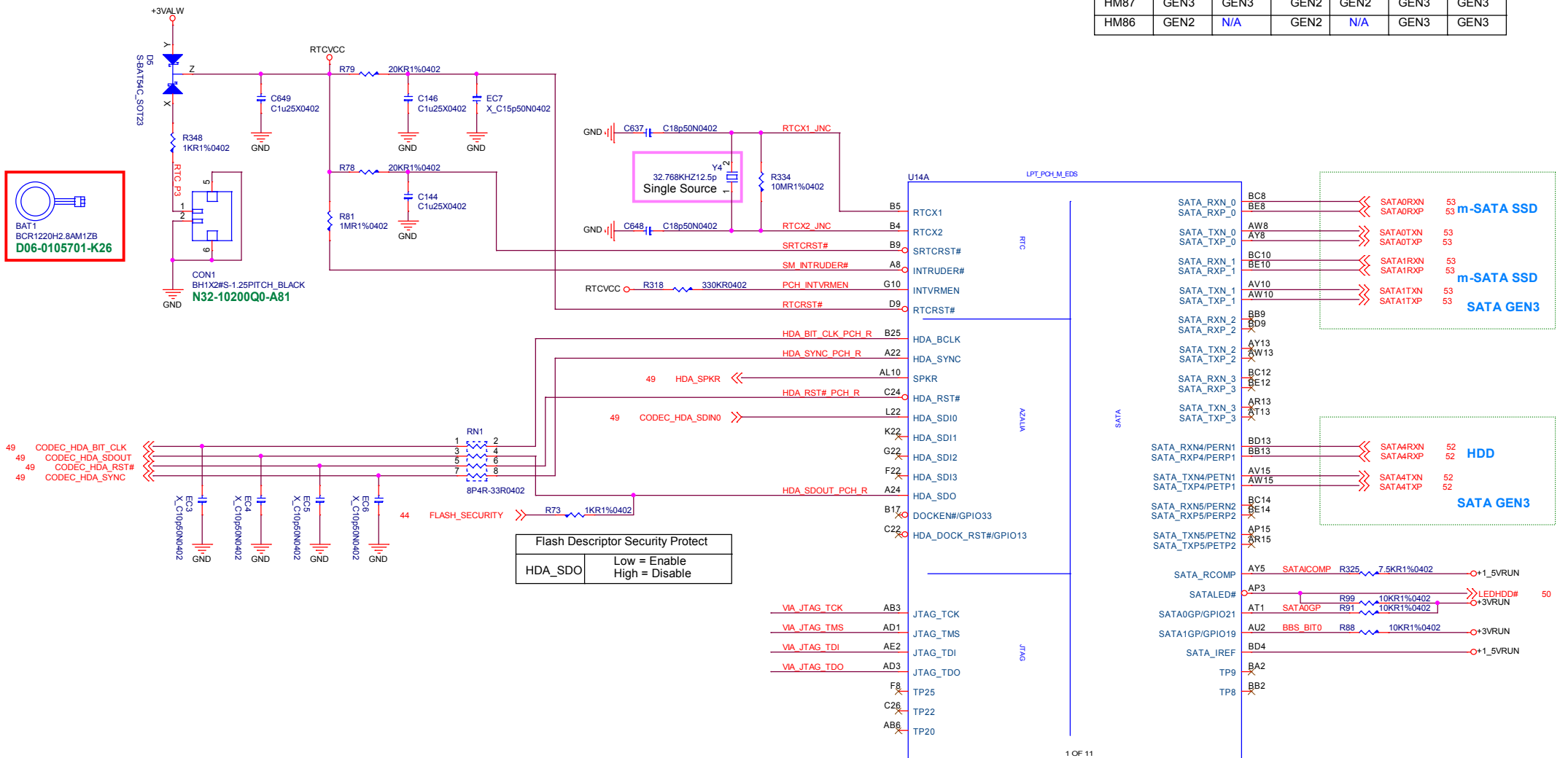


Discharge Circuit



Lynx Point (HDA/JTAG/SATA)

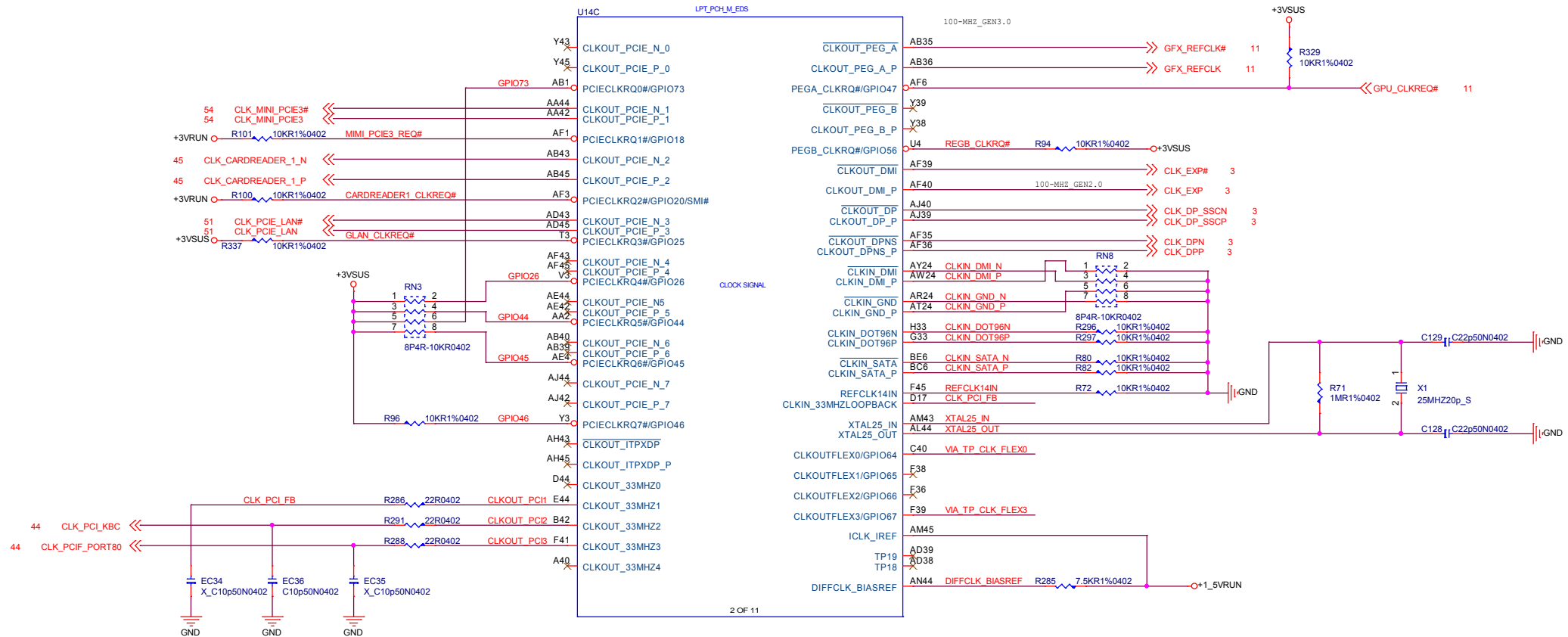
SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



SPK The Signal has a weak internal pull-down
Note: the internal pull-down is disabled after PLTRST# deasserts.
If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode
(Panther Point will disable the TCO Timer system reboot feature)

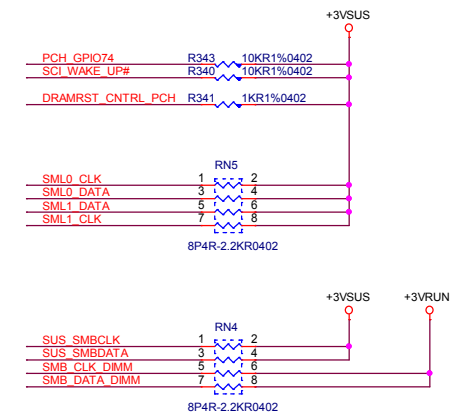
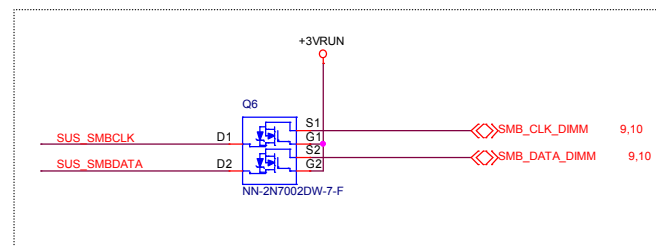
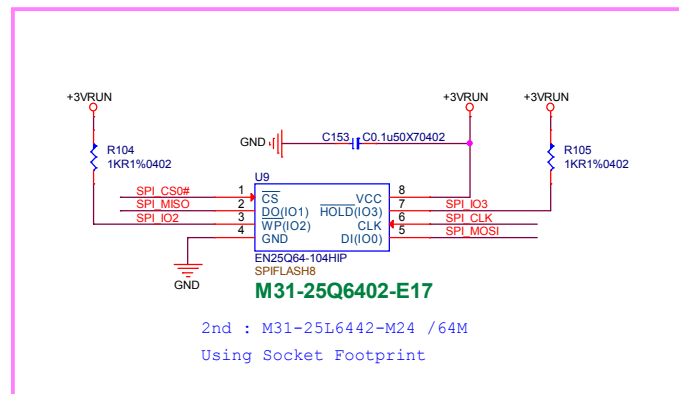
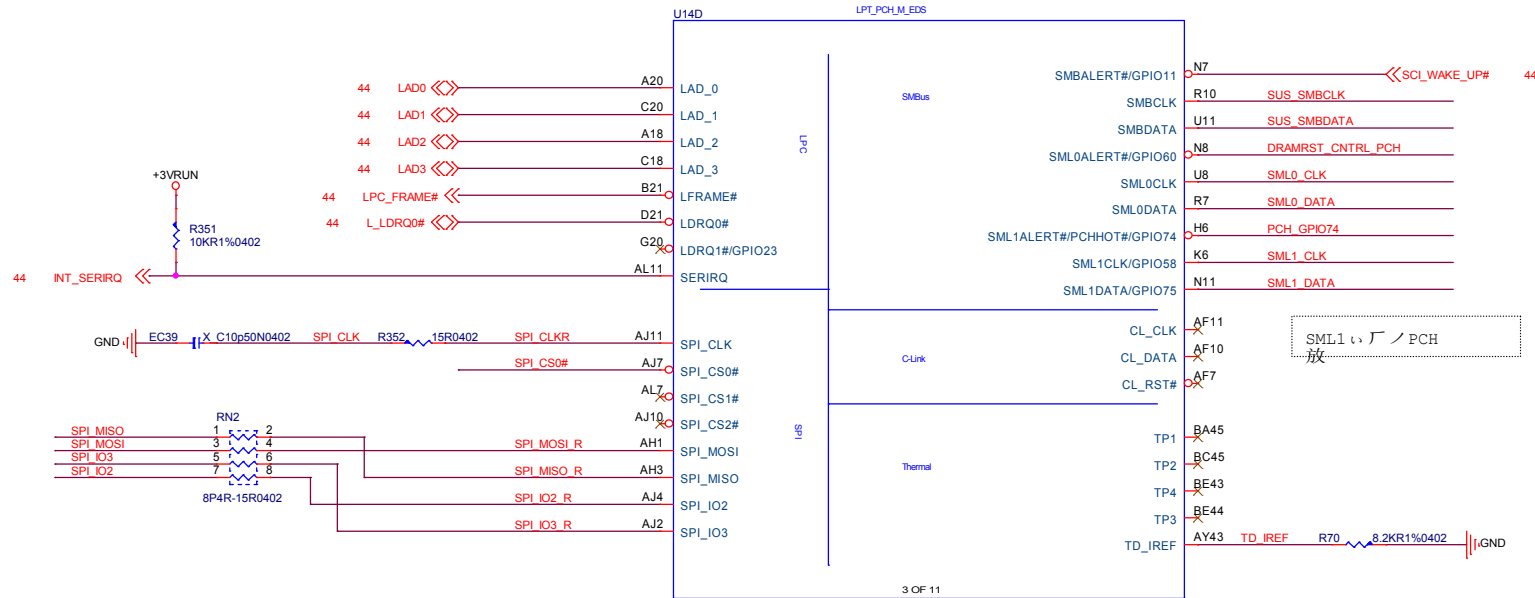
Lynx Point (Clock)

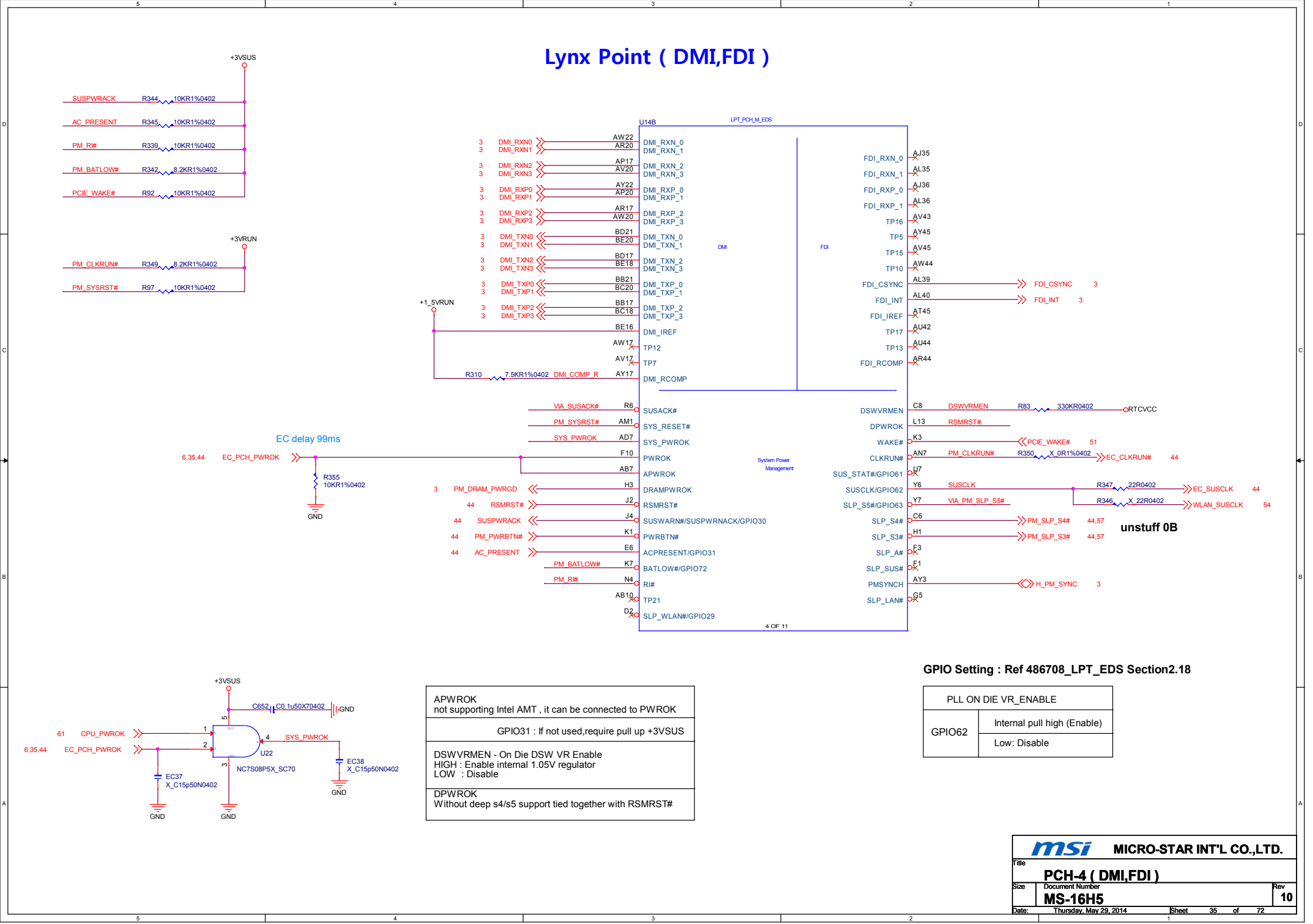
PCIE devices or add-in cards that do NOT support CLKREQ# functionality should not route this signal to PCH. Intel recommends terminating PCIE1CLKREQ# pin on PCH with 10 k Ω 10% external pull-up resistor instead of No Connect.



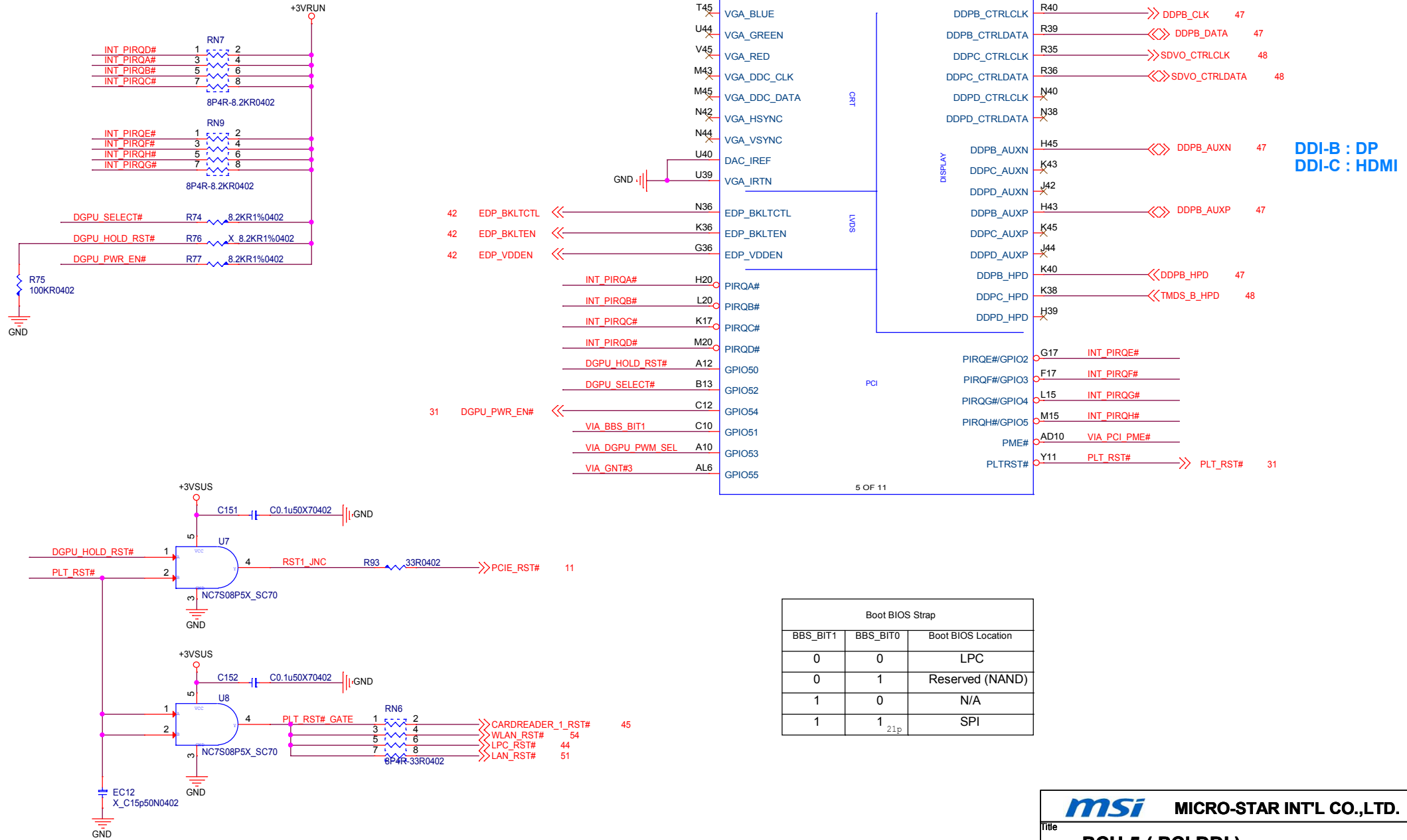
The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

Lynx Point (LPC,SMBUS)



[illegible][illegible][illegible][illegible]

Lynx Point (PCI,DDI)



5 4 3 2 1

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

U14F LPT_PCH_M_EDS

GPIO

CPU_Misc

6 OF 11

NCTF

GND

GND

GND

so 狢100R empty

PCH_THRMTRIP# R

EC9 X_C15p50N0402

msi MICRO-STAR INT'L CO.,LTD.

Title **PCH-6 (GPIO,MISC)**

Size Document Number **MS-16H5** Rev **10**

Date: Thursday, May 29, 2014 Sheet 37 of 72

5 4 3 2 1

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

U14F LPT_PCH_M_EDS

GPIO

CPU_Misc

6 OF 11

NCTF

GPIO28

Internal pull high (Enable)

Low: Disable

AN10

AY1

AT6

RCIN#

AV3

AV1

AU4

N10

A2

A41

A43

A44

B1

B2

B44

B45

BA1

BC1

BD1

BD2

BD44

BD45

BE2

BE3

D1

E1

E45

A4

R317 10KR1%0402

R320 10KR1%0402

R338 10KR1%0402

R314 10KR1%0402

R98 10KR1%0402

R95 X 10KR1%0402

R87 X_1KR1%0402

R86 390R0402

X_1KR1%0402

X_C15p50N0402

EC9

so 100R empty

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PCH-6 (GPIO,MISC)

Document Number

MS-16H5

Date: Thursday, May 29, 2014

Sheet 37 of 72

Rev 10

5 4 3 2 1

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

U14F LPT_PCH_M_EDS

GPIO

6 OF 11

CPUMisc

NCTF

TP14 AN10 AY1 VIA_PECI RCIN# AT6 AV3 PROCPWRGD THRMTRIP# AV1 PCH_THRMTRIP#_R R86 390R0402 PLTRST_PROC# AU4 VSS N10

VSS A2 A41 A43 A44 B1 B2 B44 B45 BA1 BC1 BD1 BD2 BD44 BD45 BE2 BE3 D1 E1 E45 A4

GND

GND

GND

EC9 X_C15p50N0402

そ 獅100R empty

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

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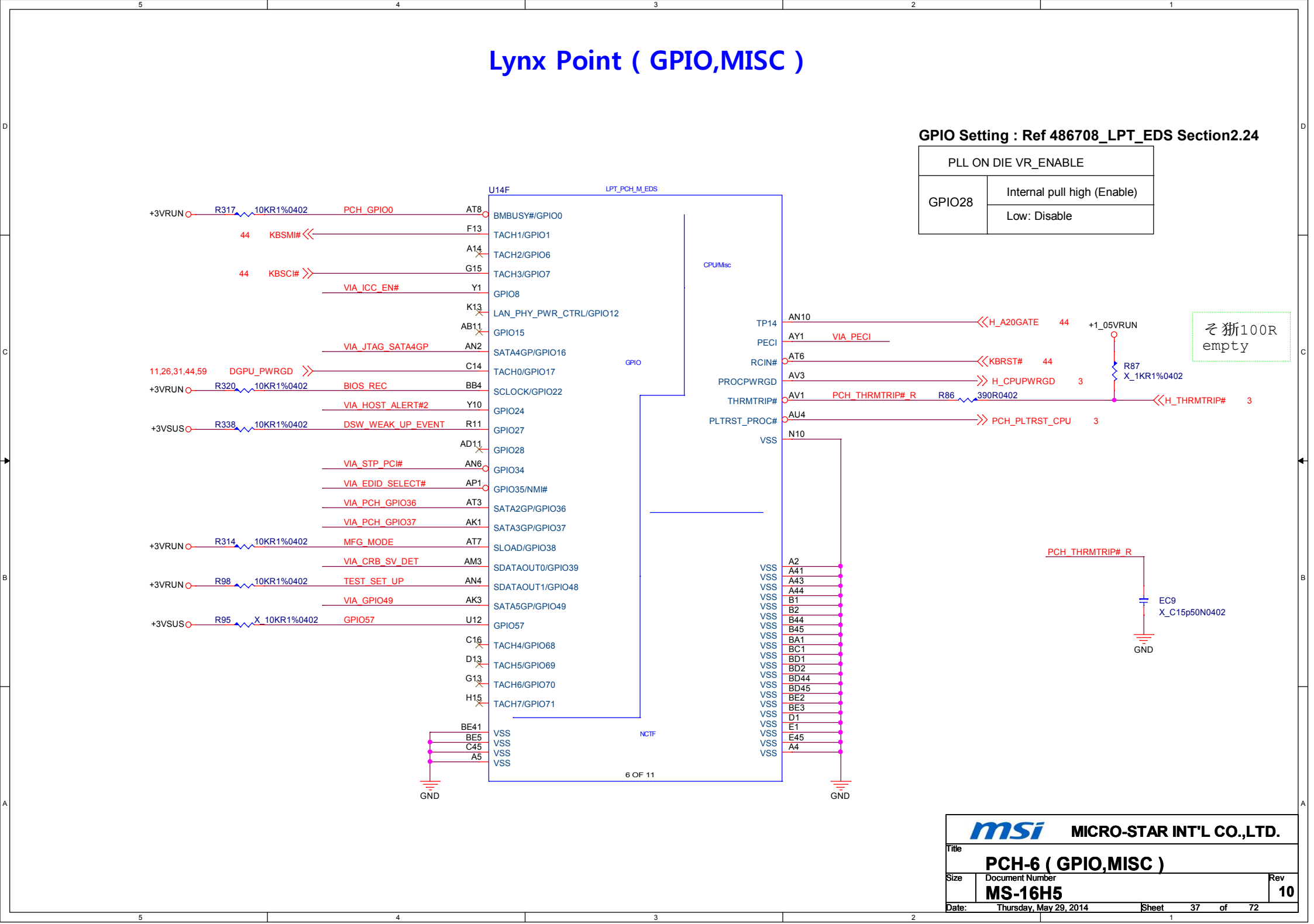
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Size Document Number MS-16H5

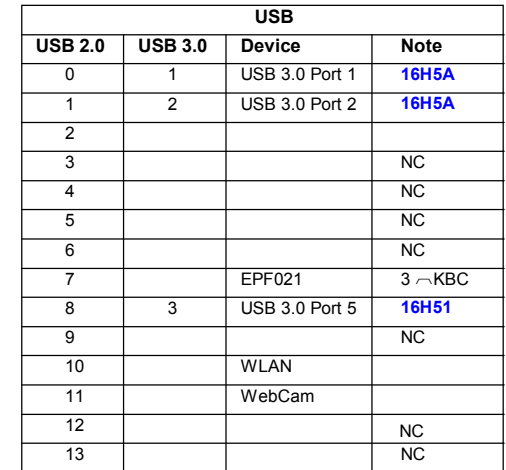
Date: Thursday, May 29, 2014

Sheet 37 of 72

Rev 10

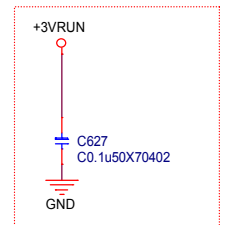
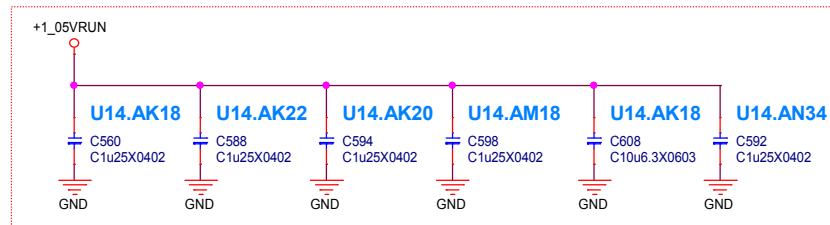
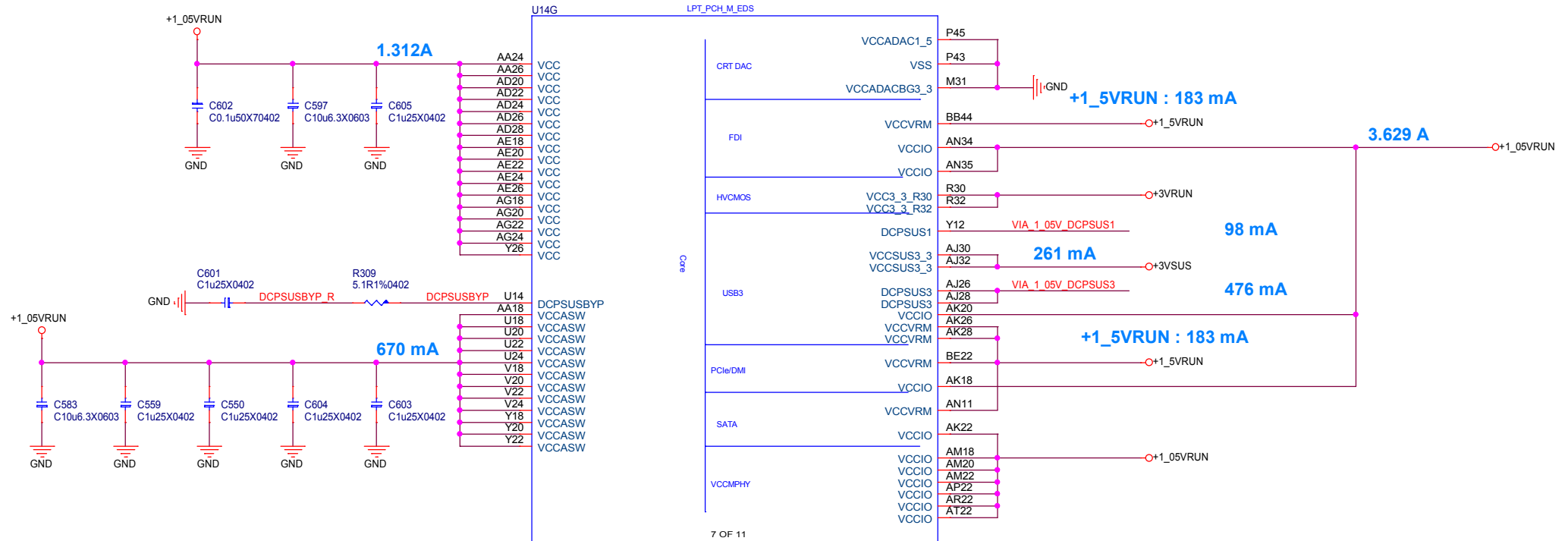


Intel Lynx Point ECHI USB(2.0) debug transport 惠钒Port1 or Port9

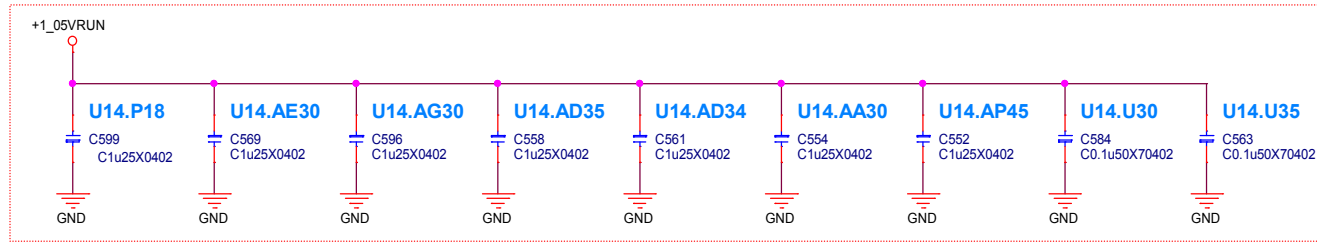
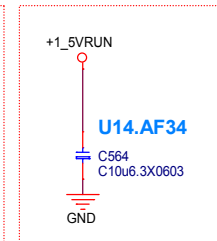
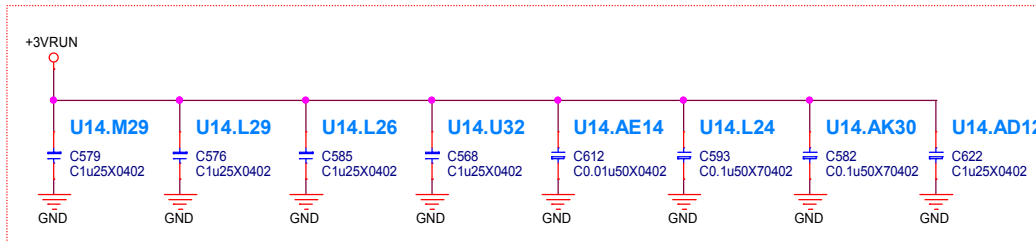
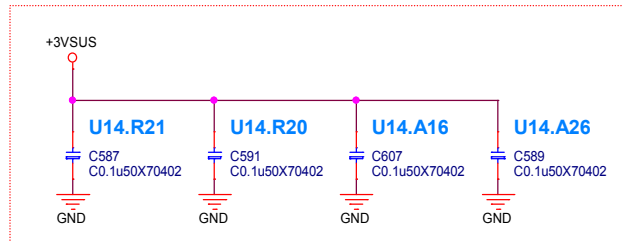
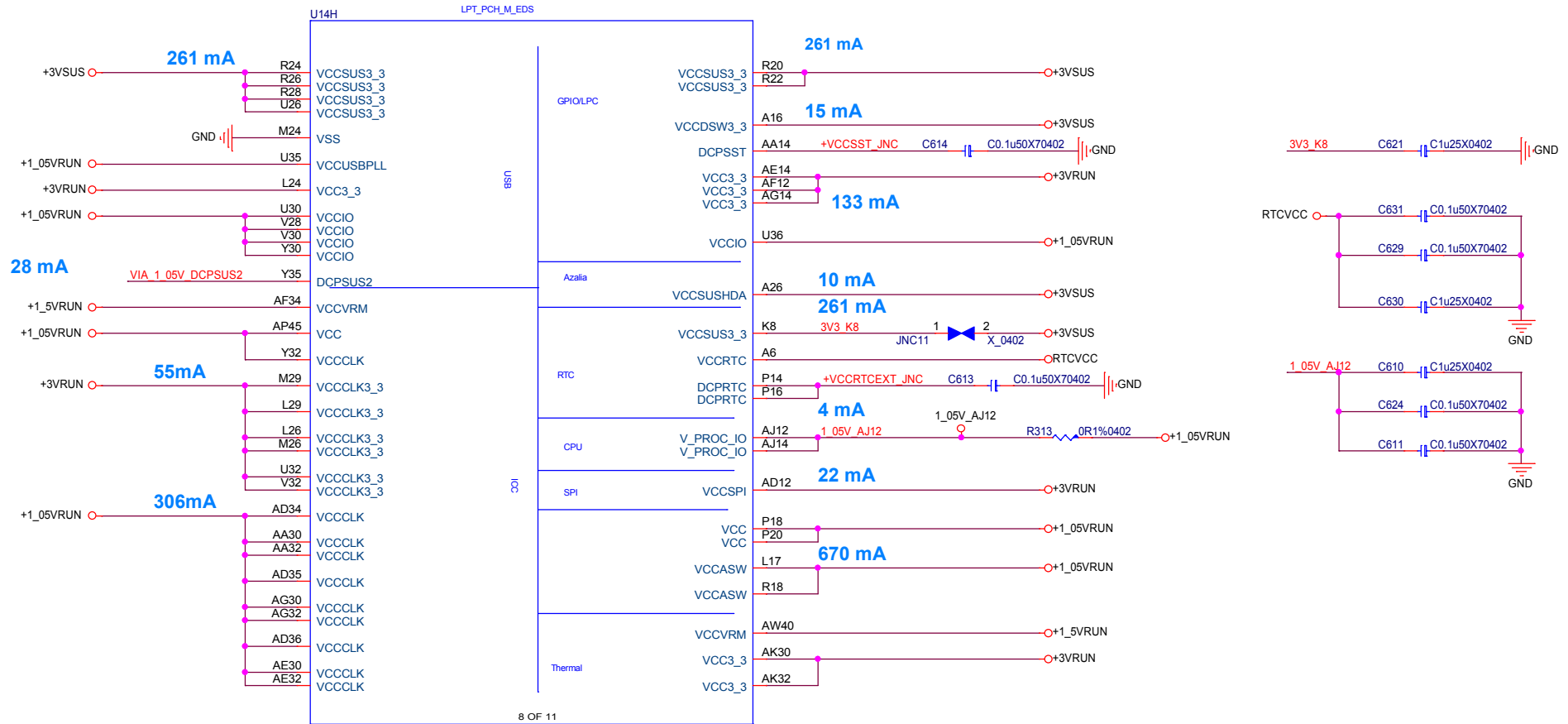


HM86 Δ USB3.0 PORT 5,6

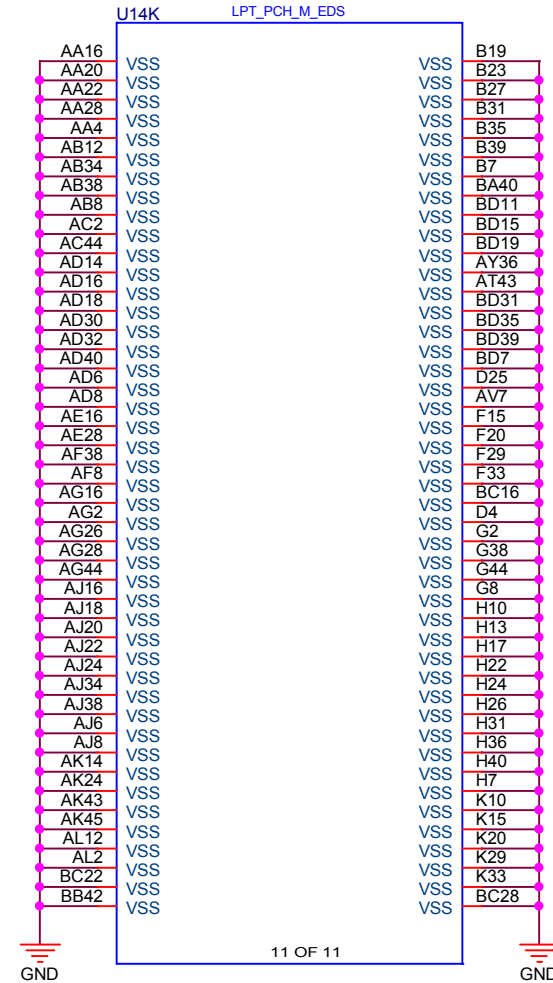
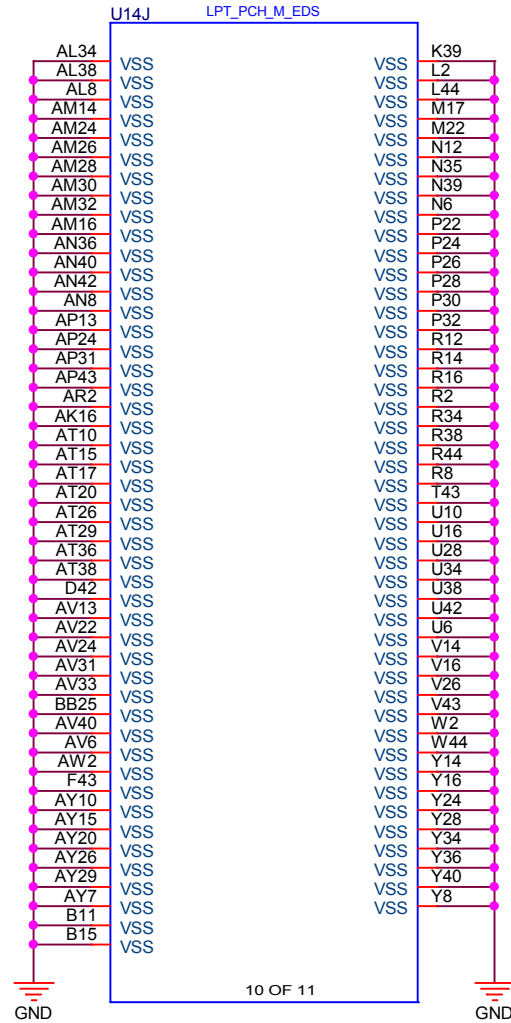
Lynx Point (Power)



Lynx Point (Power)



Lynx Point (GND)

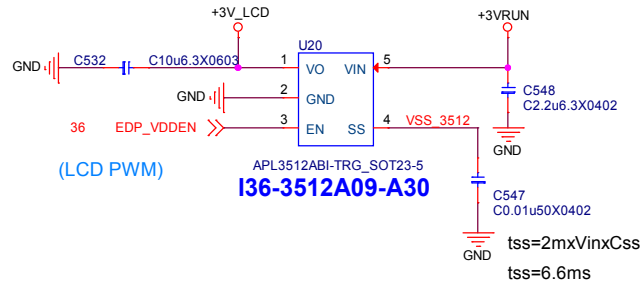


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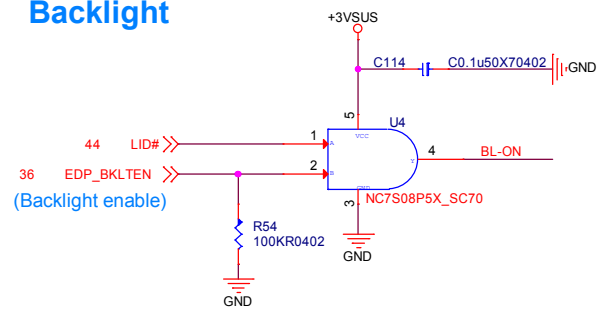
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PCH-8 (GND)		
Size	Document Number	Rev
	MS-16H5	10
Date:	Thursday, May 29, 2014	Sheet 41 of 72

eDP Connector

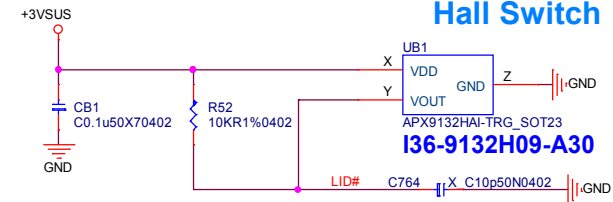
Pannel Device Logic Power



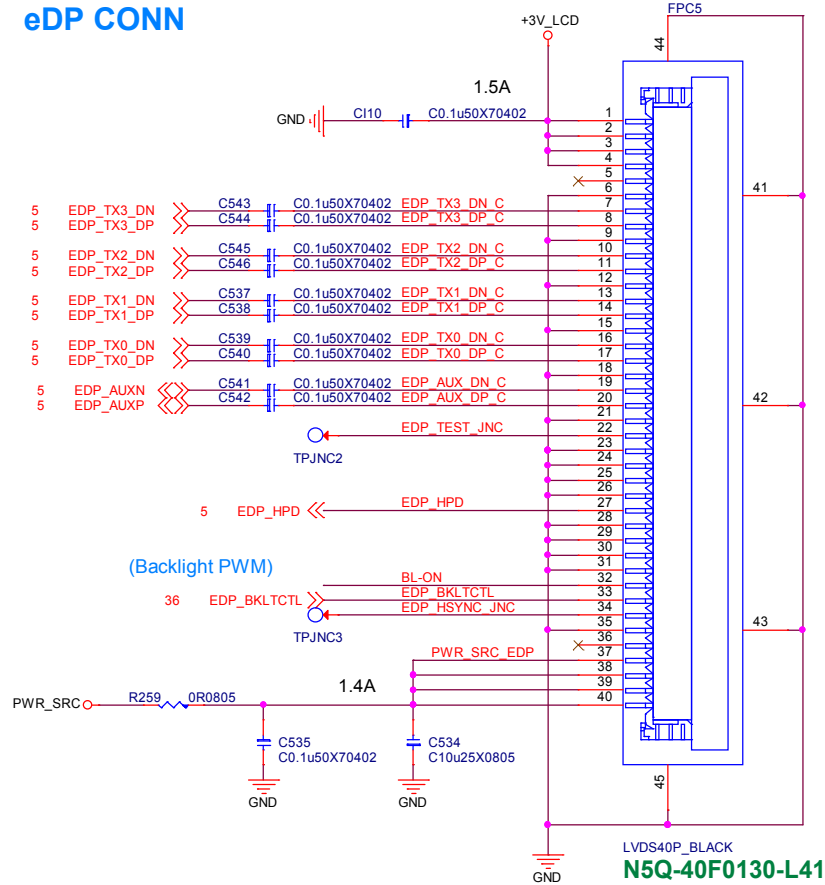
Backlight



Hall Switch



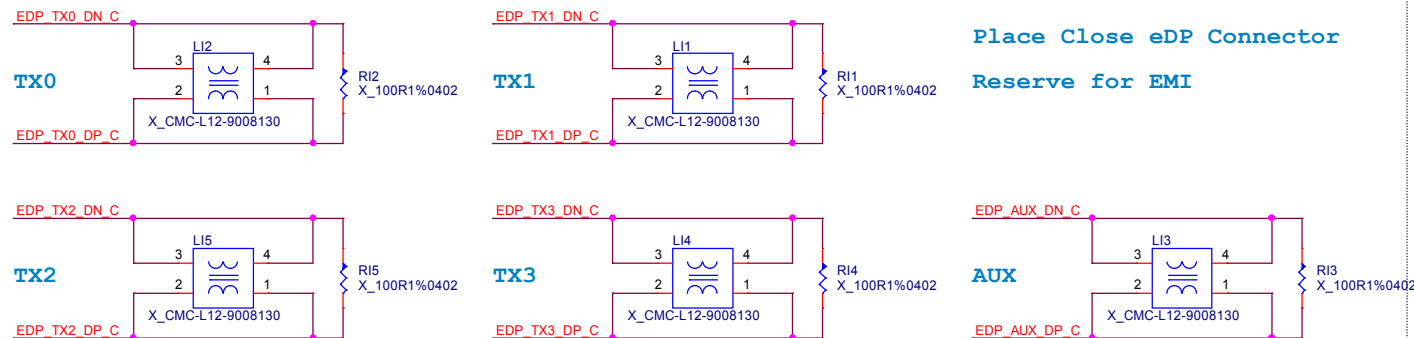
eDP CONN



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPDP signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

Place Close eDP Connector
Reserve for EMI

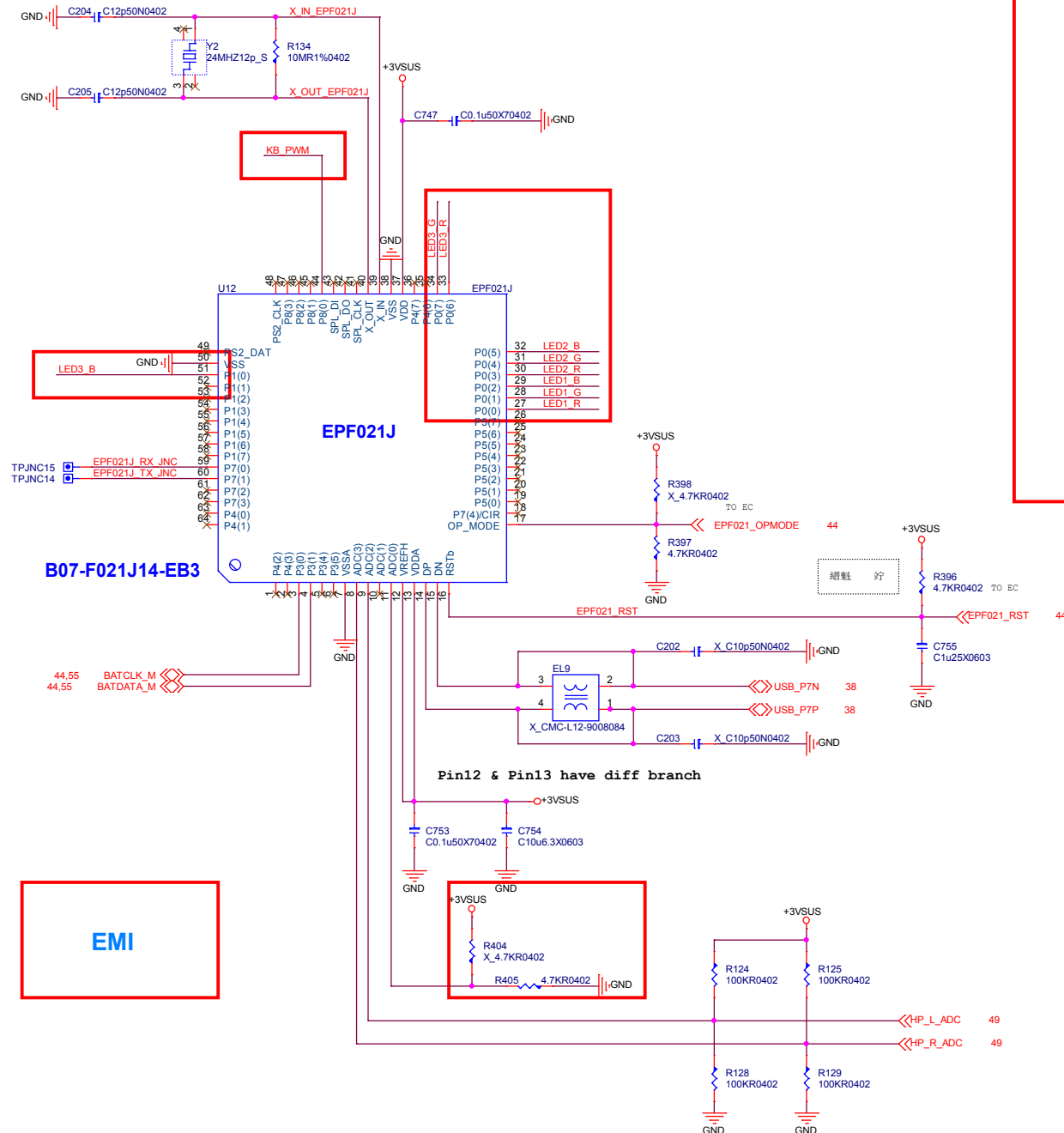


msi

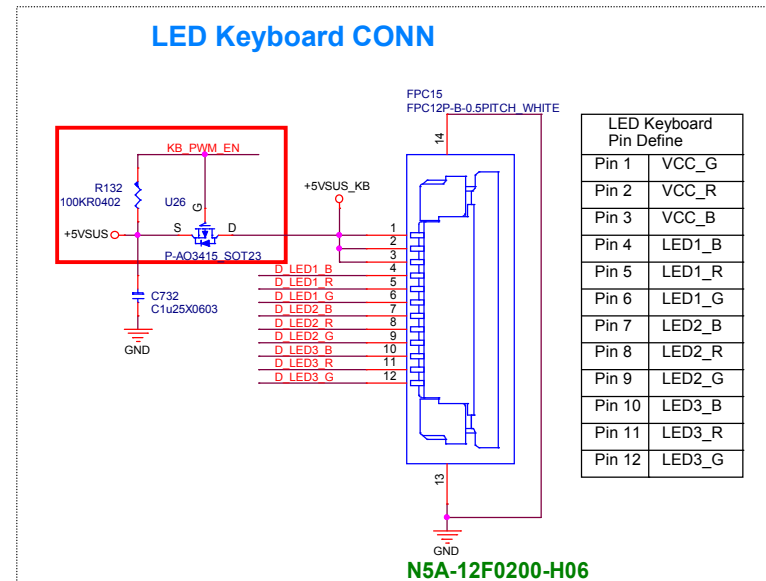
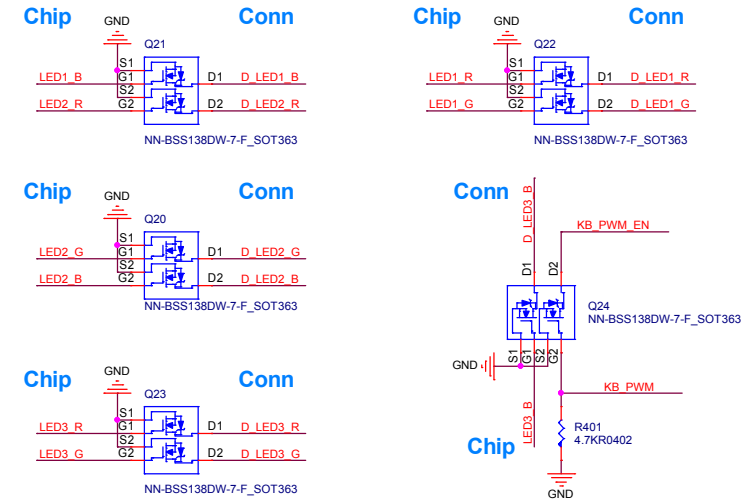
MICRO-STAR INT'L CO.,LTD.

Title eDP Connector		
Size	Document Number MS-16H5	Rev 10
Date:	Thursday, May 29, 2014	Sheet 42 of 72

LED 8051 Controller



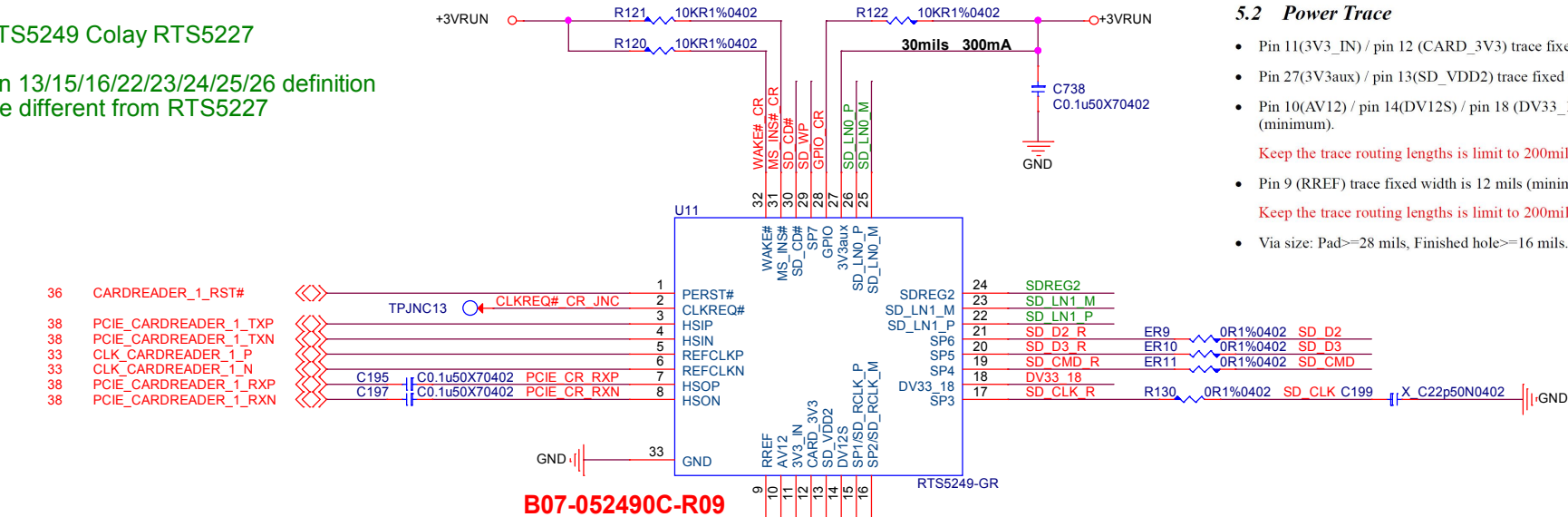
EPF021J Sink current not enough, only using BSS138 (0.22A)



CardReader (RTS5249)

RTS5249 Colay RTS5227

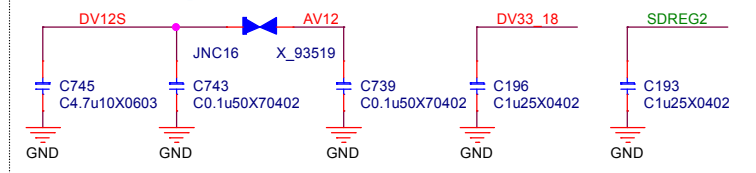
Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227



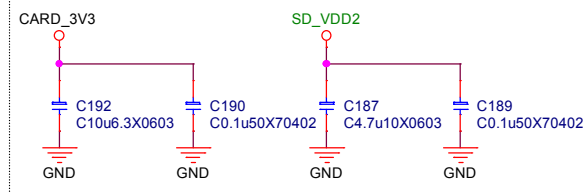
5.2 Power Trace

- Pin 11(3V3_IN) / pin 12 (CARD_3V3) trace fixed width is 40 mils (minimum).
- Pin 27(3V3aux) / pin 13(SD_VDD2) trace fixed width is 30 mils (minimum).
- Pin 10(AV12) / pin 14(DV12S) / pin 18 (DV33_18) / pin 24(SDREG2) trace fixed width is 20 mils (minimum).
- Keep the trace routing lengths is limit to 200mils.
- Pin 9 (RREF) trace fixed width is 12 mils (minimum).
- Keep the trace routing lengths is limit to 200mils.
- Via size: Pad>=28 mils, Finished hole>=16 mils.

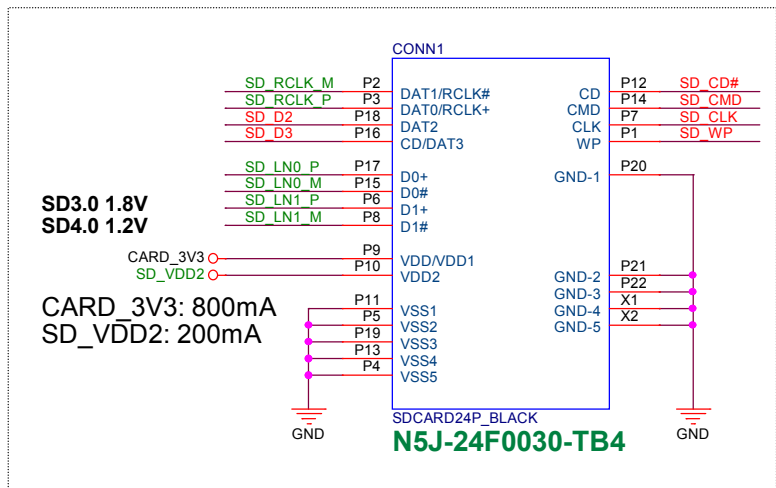
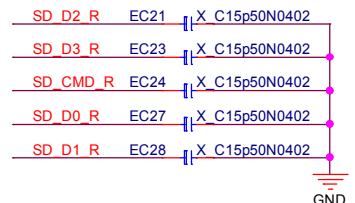
Close Chip



Close Connector



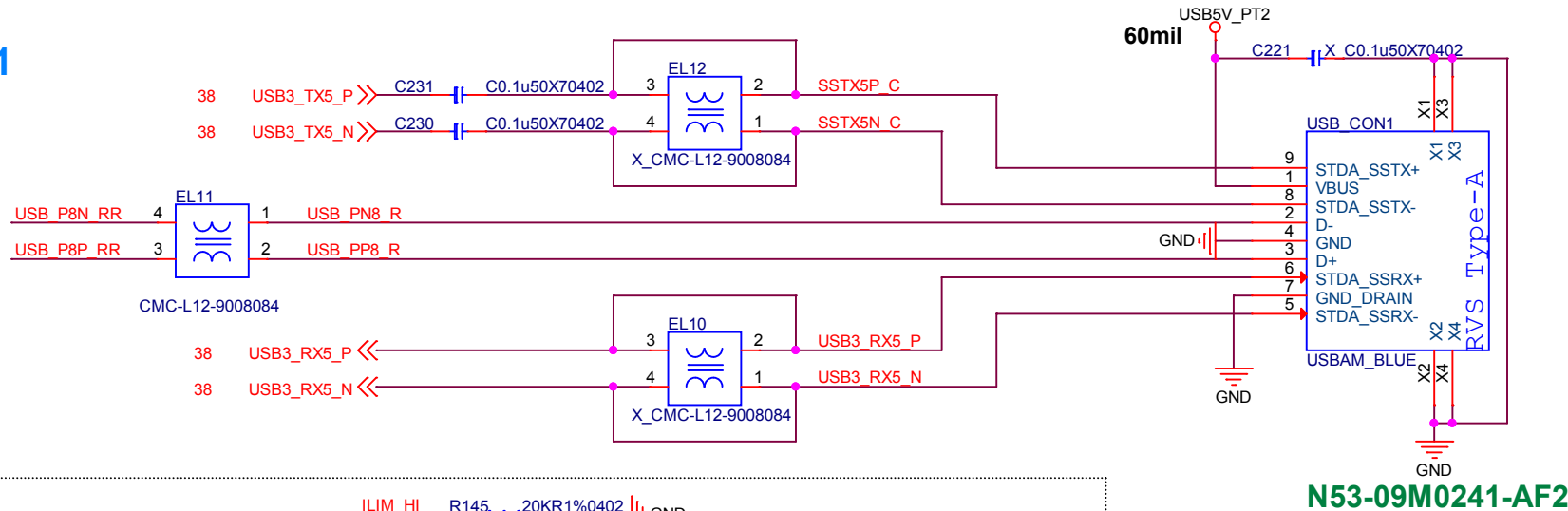
EMI



USB 3.0 / iCharger

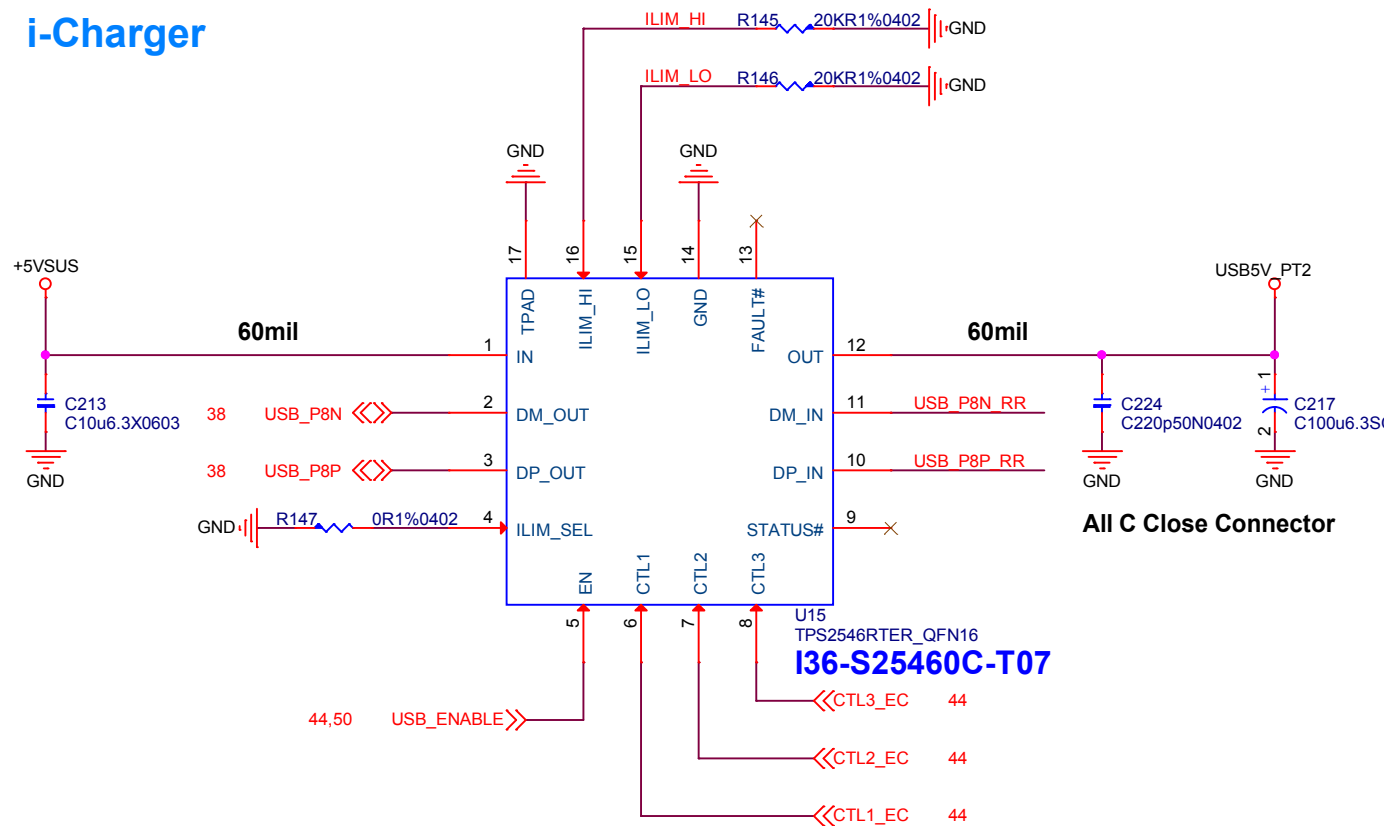
USB3.0 CNT-1

USB3.0 Port-6
USB2.0 Port-9



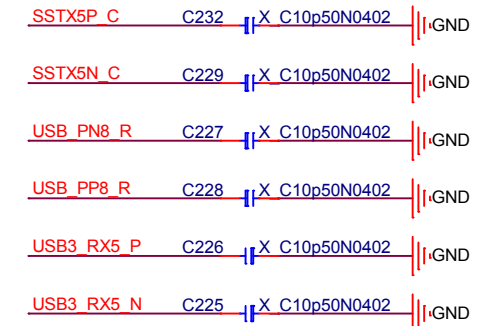
N53-09M0241-AF2

i-Charger



All C Close Connector

EMI

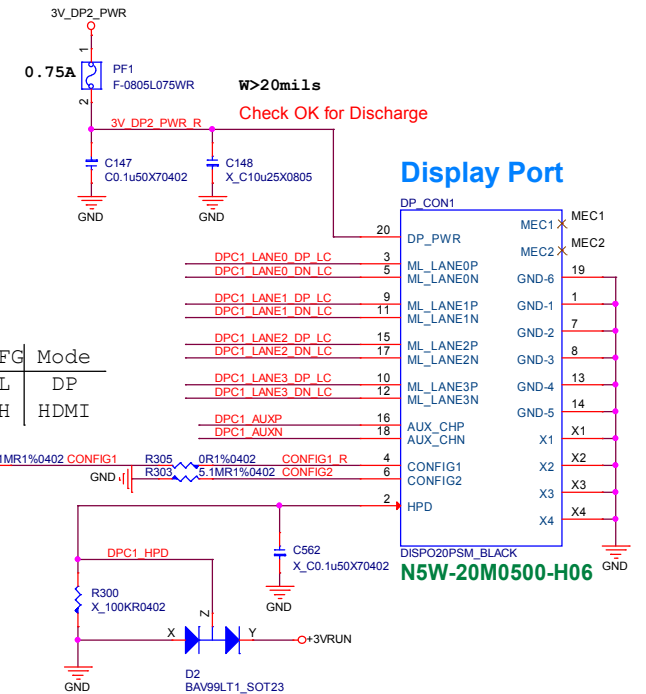
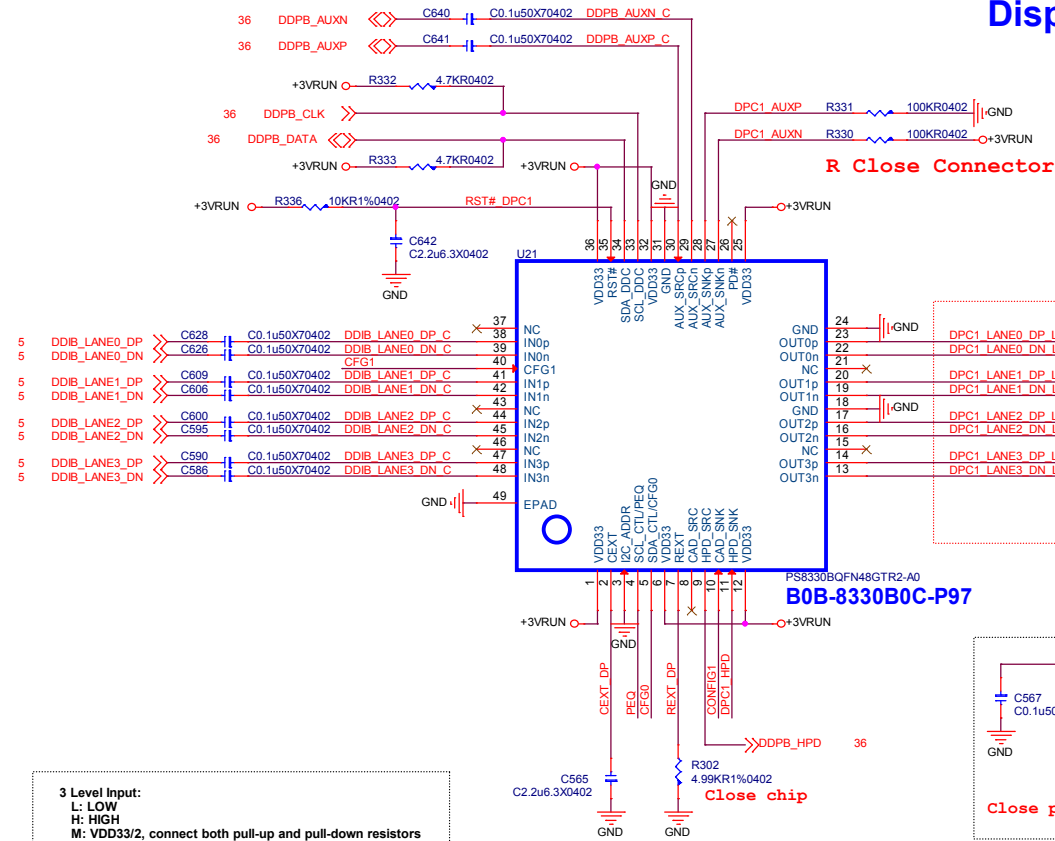


msi

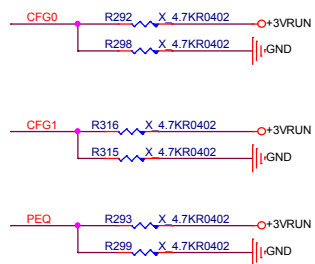
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Title			USB 3.0 / iCharger	
Size	Document Number		Rev	
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Display Port



CAD_SNK Have internal Pull down 1Mohm.
HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the
box-to-box connectors must support the
maximum current rating of 500mA.



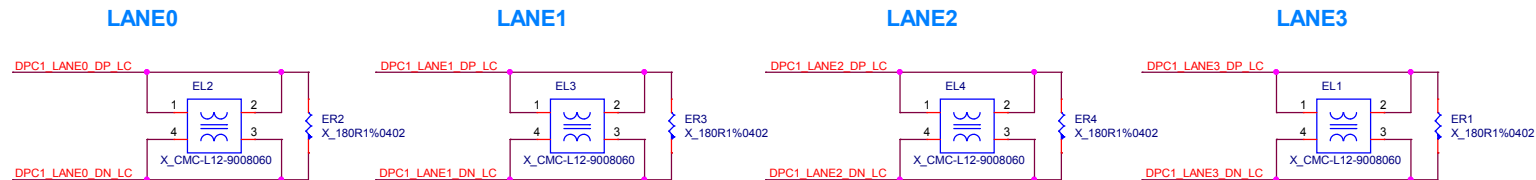
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
 L: default, automatic EQ enable & AUX interception enable
 M: automatic EQ disable & AUX interception enable
 N: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

```
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable
```

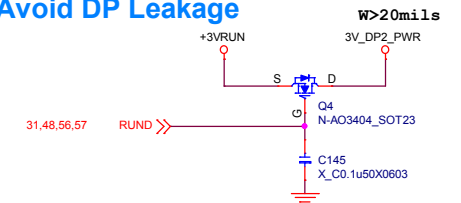
Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.

- L: default, LEQ, compensate channel loss up to 12dB @ HBR2
- H: HEQ, compensate channel loss up to 15dB @ HBR2
- M: LLEQ, compensate channel loss up to 5dB @ HBR2

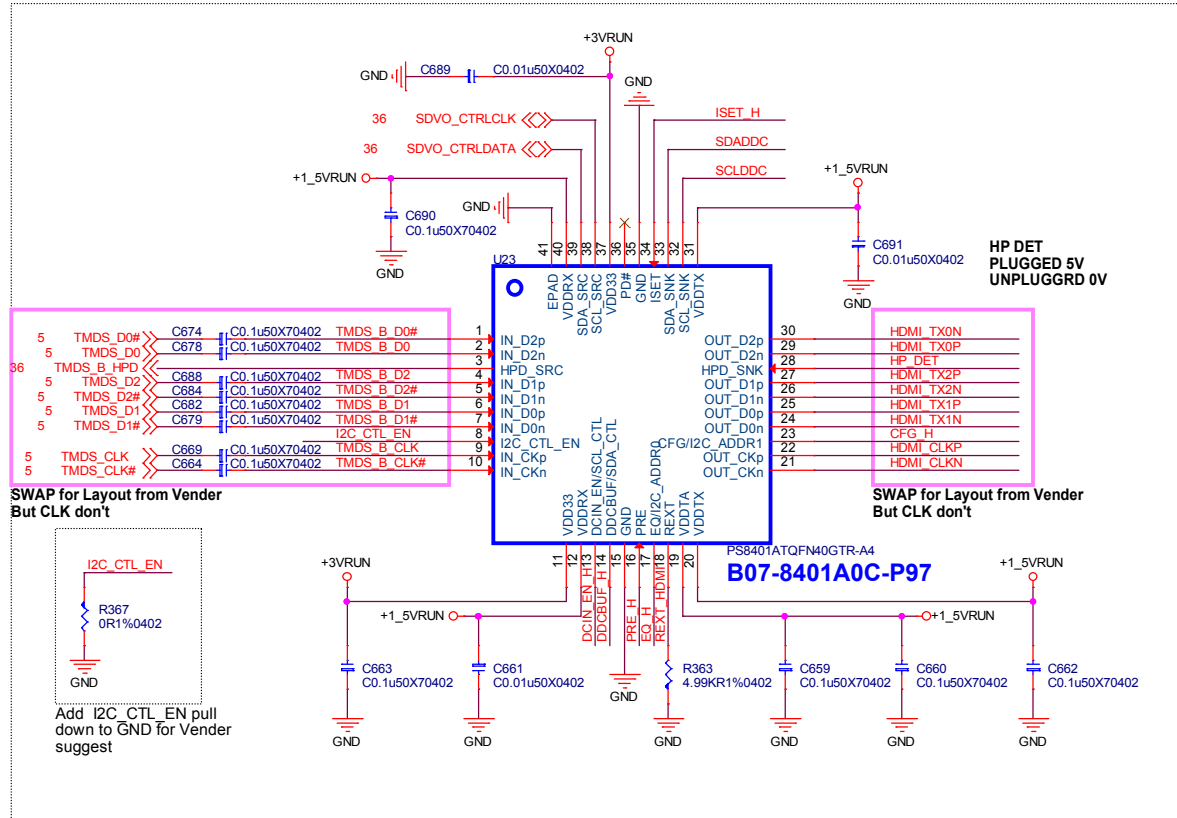
EMI Close Connector



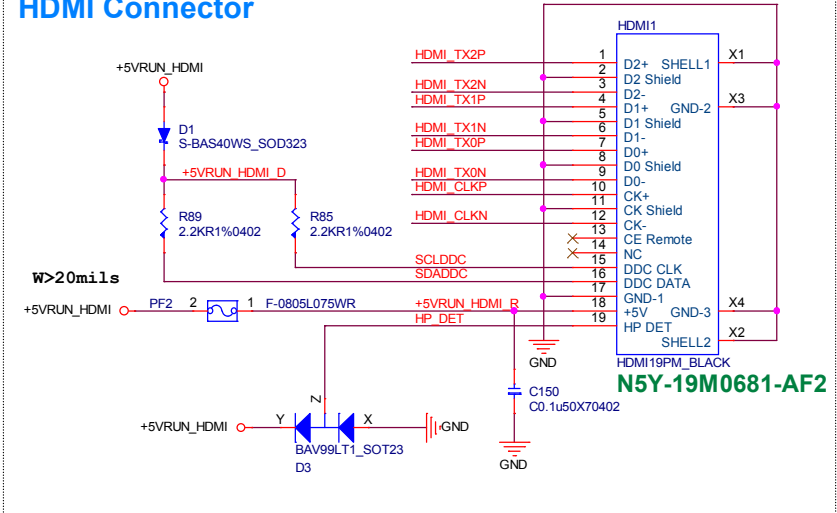
Avoid DP Leakage



HDMI Repeater



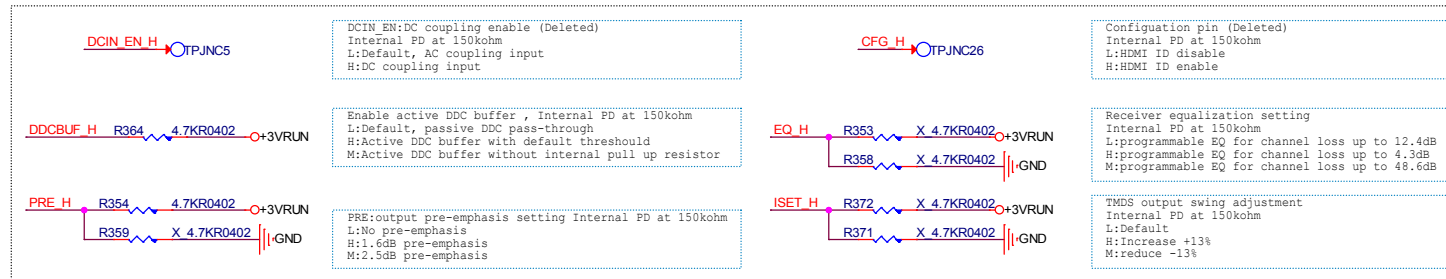
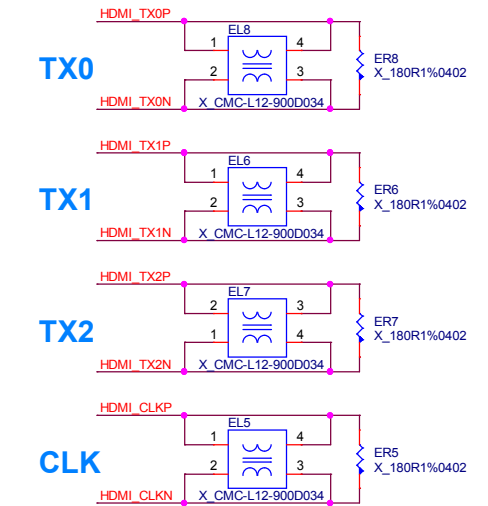
HDMI Connector



An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

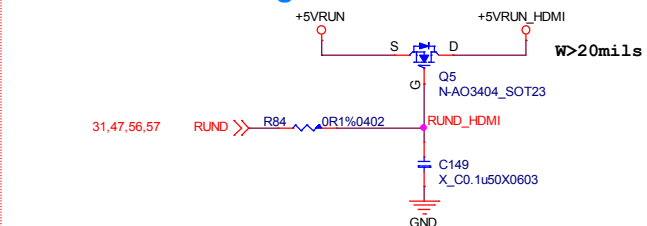
HPD_SNK Internal PD 150kohm

EMI Close Connector

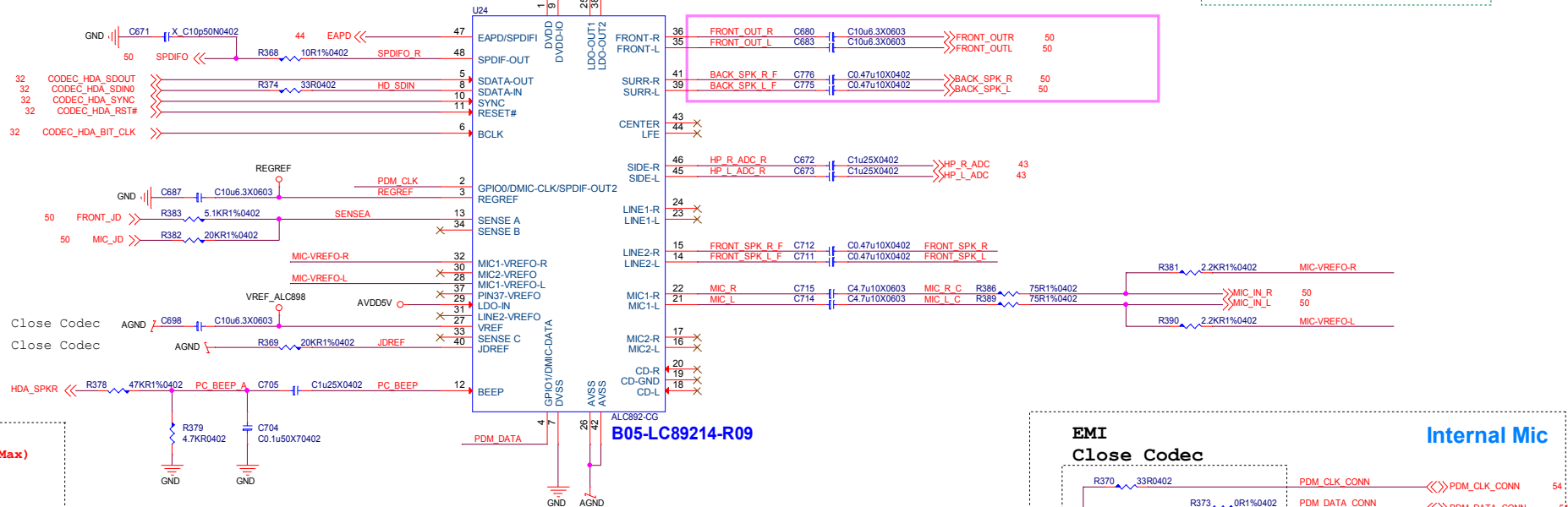
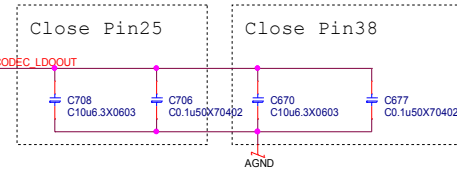
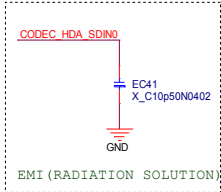


ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150k , 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

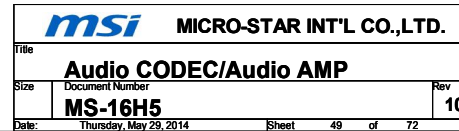
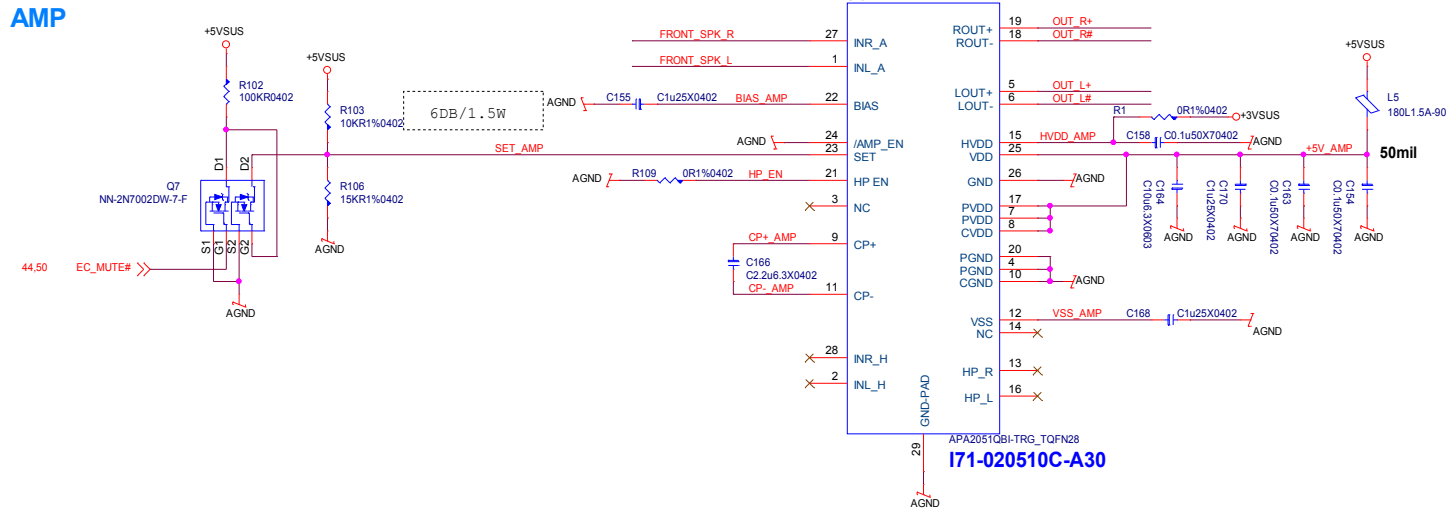
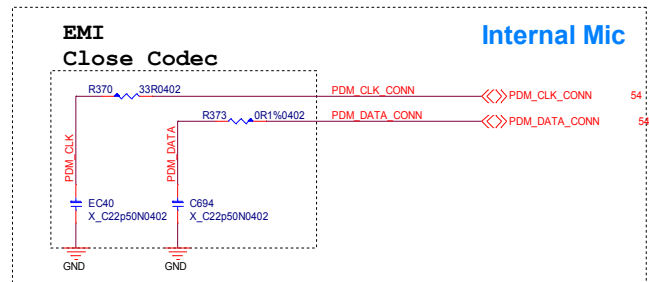
Avoid HDMI Leakage



Audio CODEC/Audio AMP

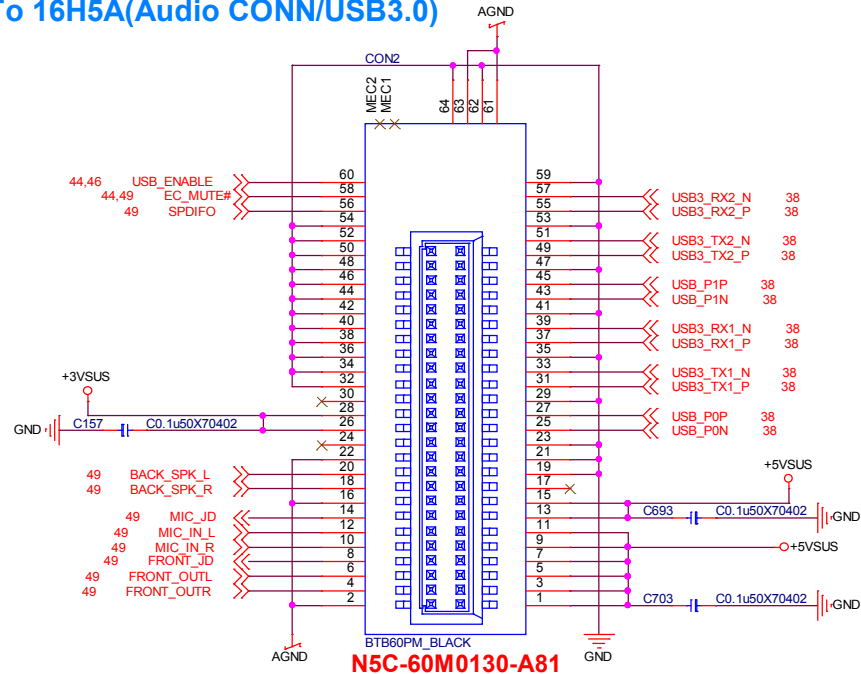


For 6dB When Using 1.5W (Normal)
(R103:10Kohm, R106:15Kohm)

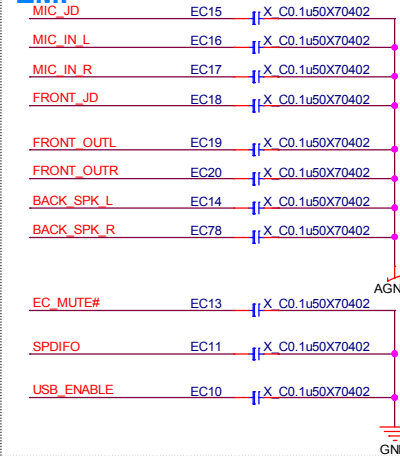


CPU FAN/BTB CONN

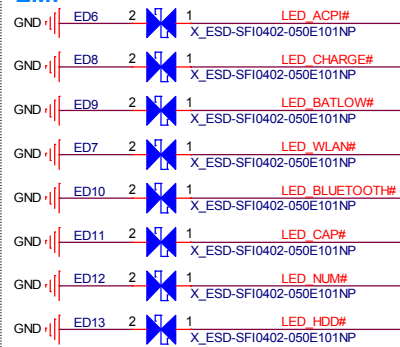
To 16H5A(Audio CONN/USB3.0)



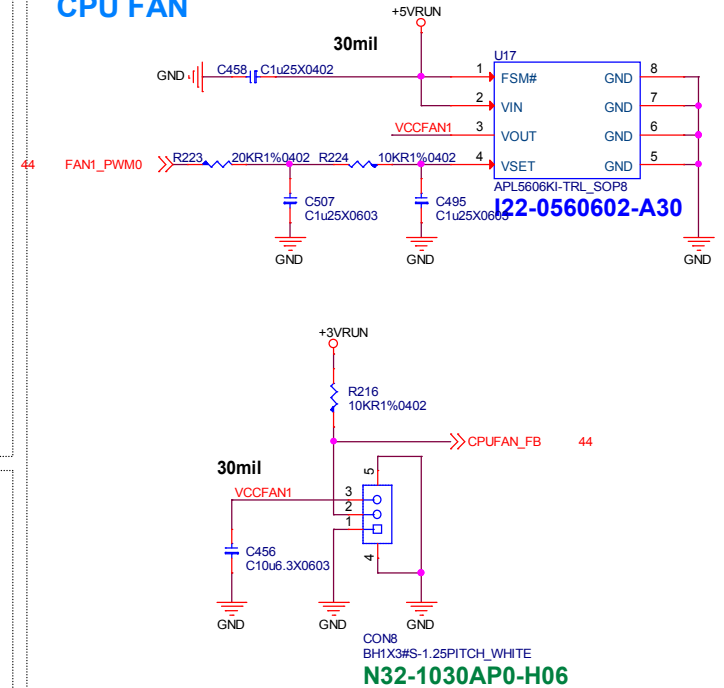
EMI



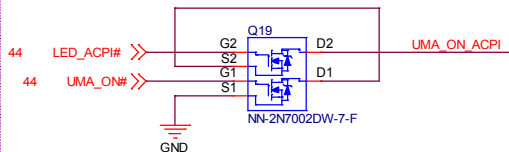
EMI



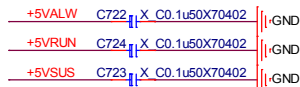
CPU FAN



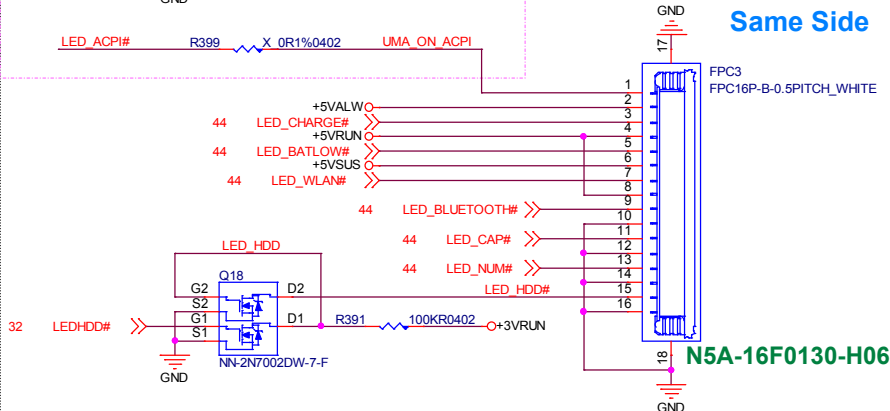
S3 Breath S0 No active



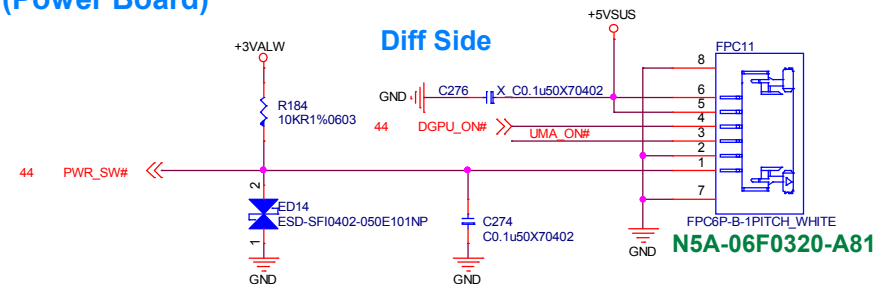
To 16H5B(LED Board)



Same Side



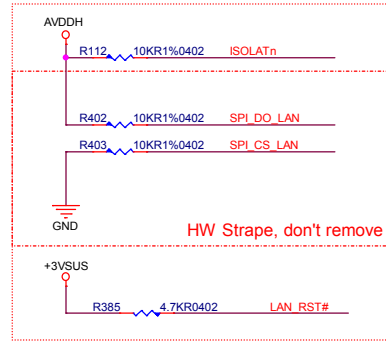
To 16H5C (Power Board)



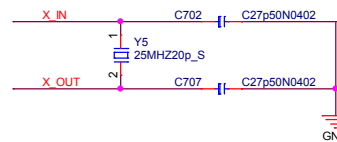
msi

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GIGA LAN(BigFoot BFN2205B)

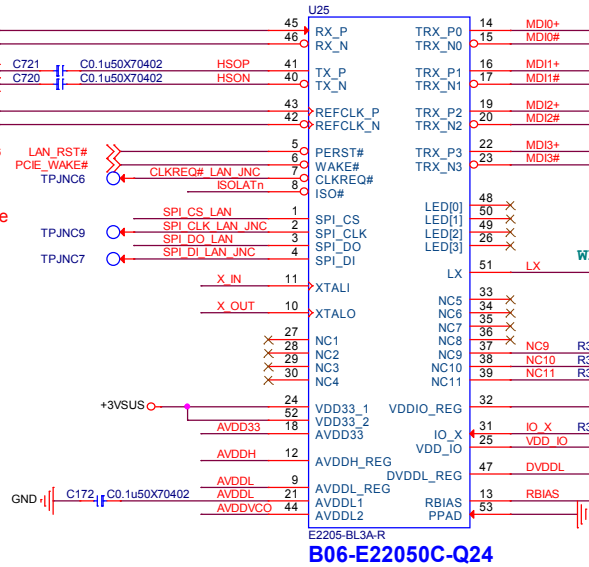
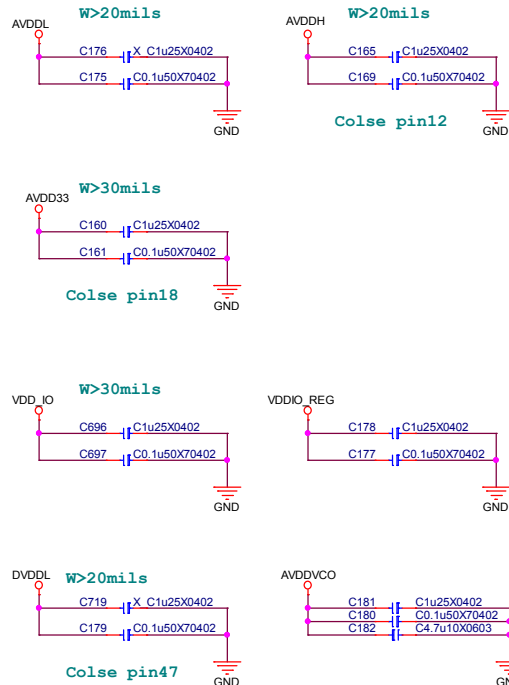


RST# spacing 20mils



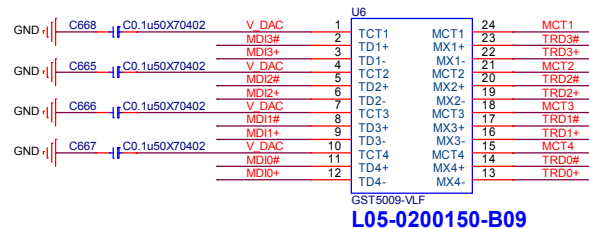
For LAN lost issue

Power CAP

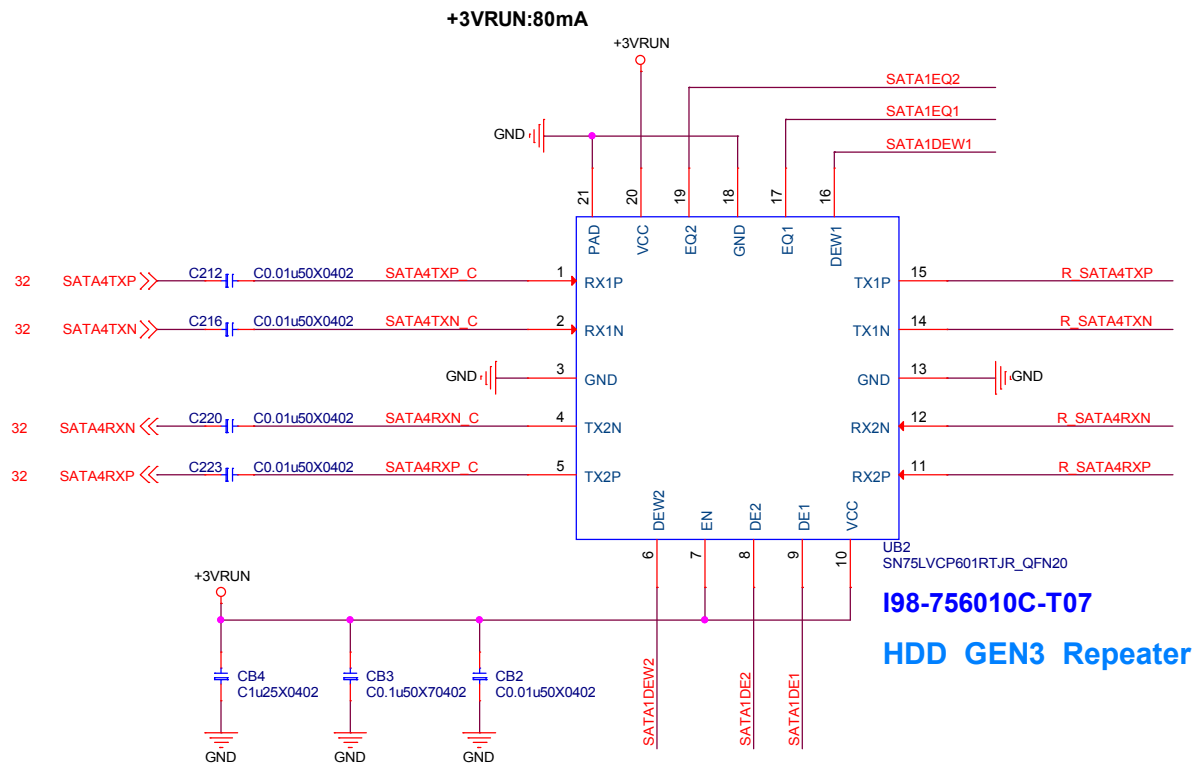


B06-E22050C-Q24

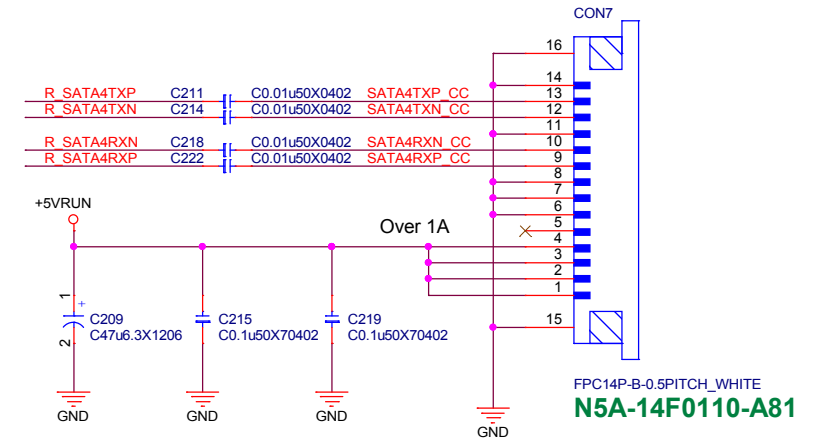
MAC 網 CHIP
す, 201



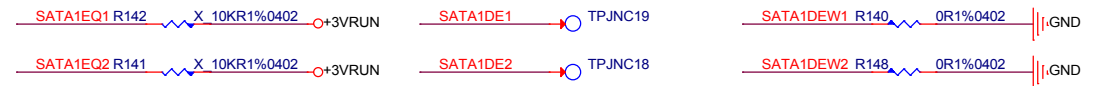
HDD (With Repeater)



BTB Connector



TI SN75LVCP601RTJR HW Setting



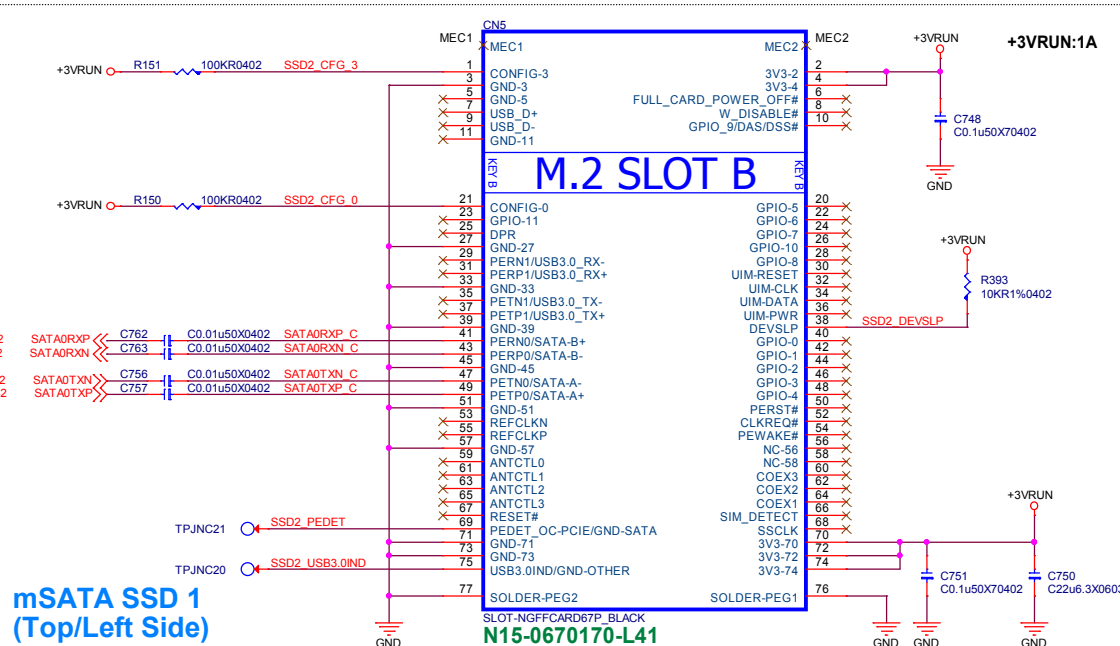
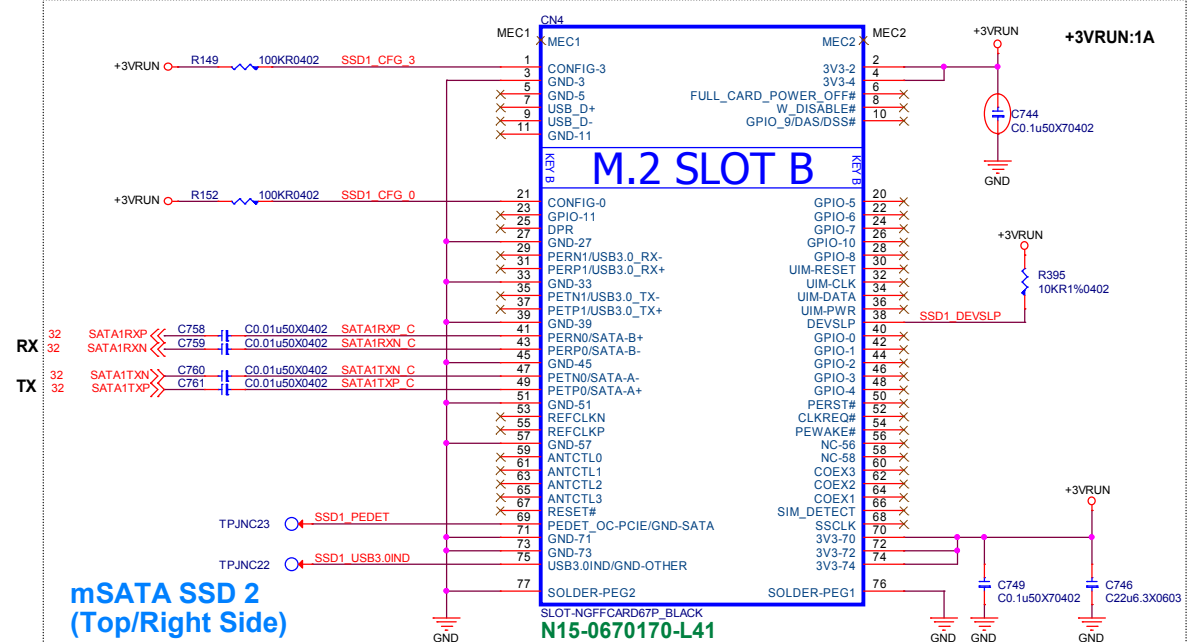
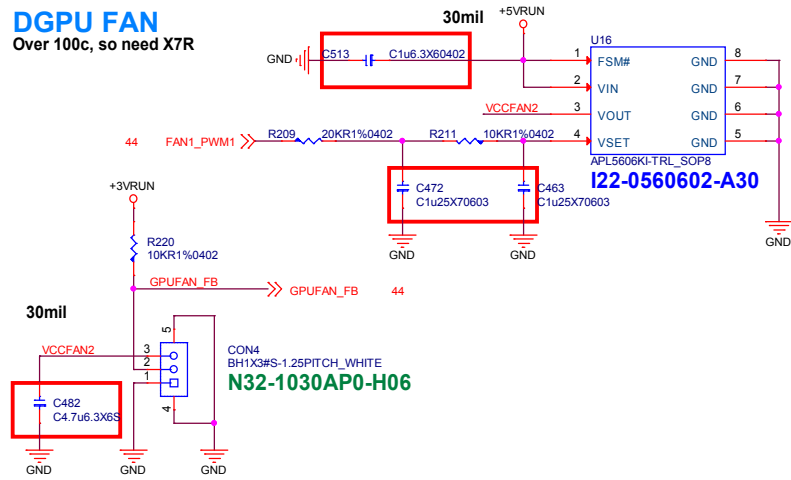
DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (<i>default</i>)	−4	NC (<i>default</i>)	0
0	0	0	7
1	−2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (<i>default</i>)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

SSD/ DGPU FAN

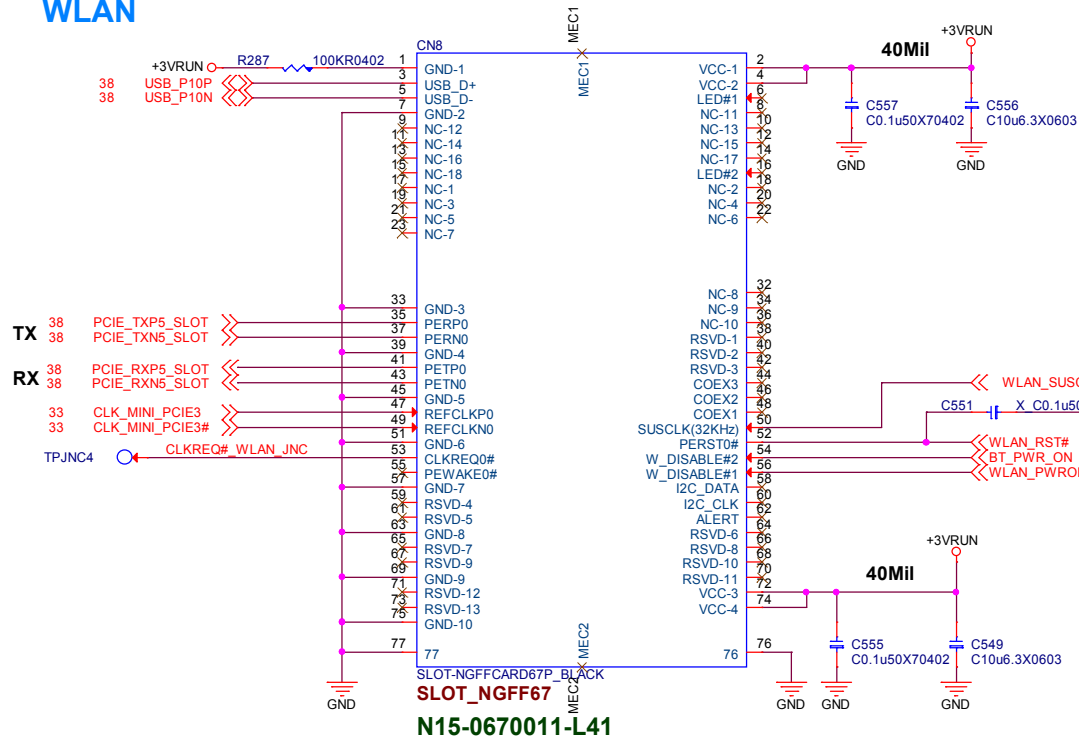
DGPU FAN

Over 100c, so need X7R

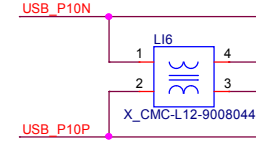


40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

WLAN

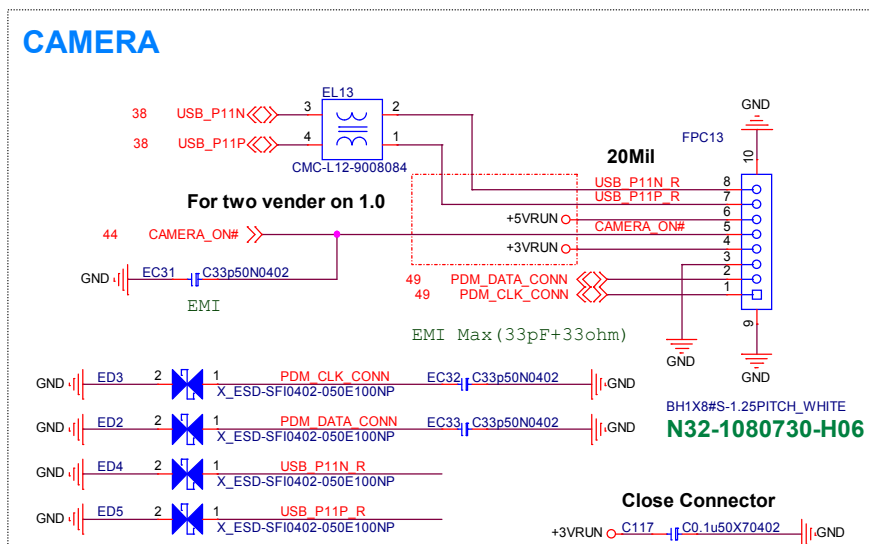


EMI

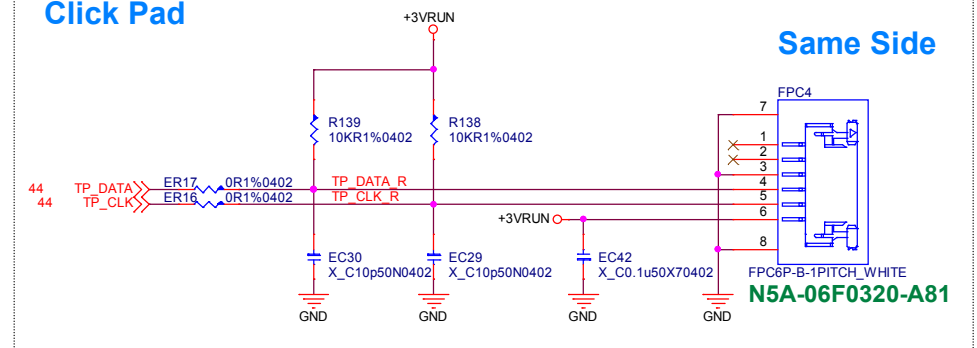


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN(W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

CAMERA

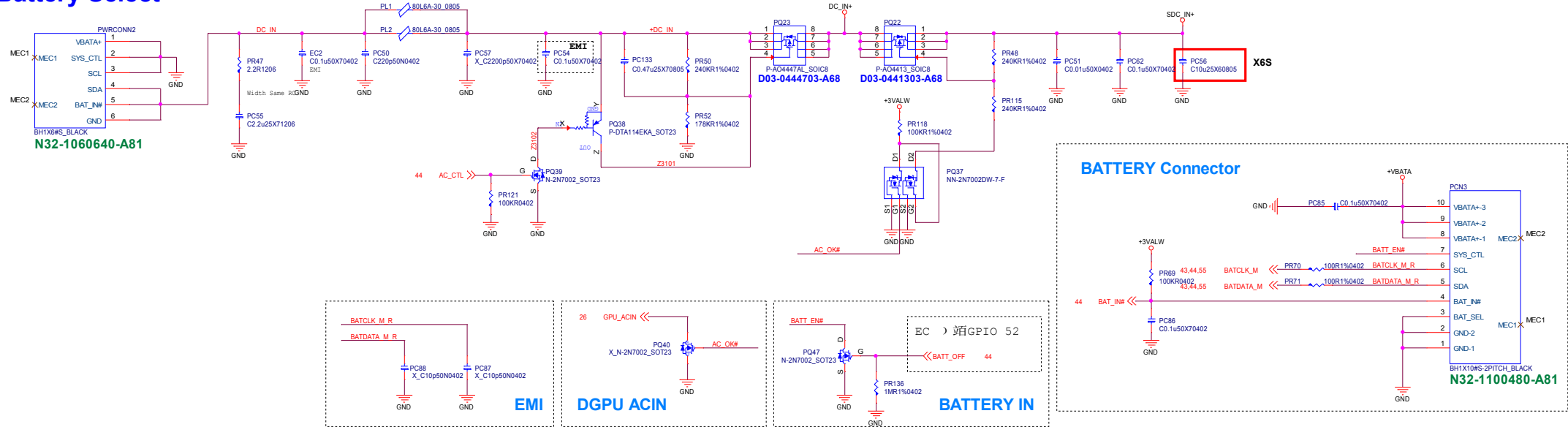


Click Pad

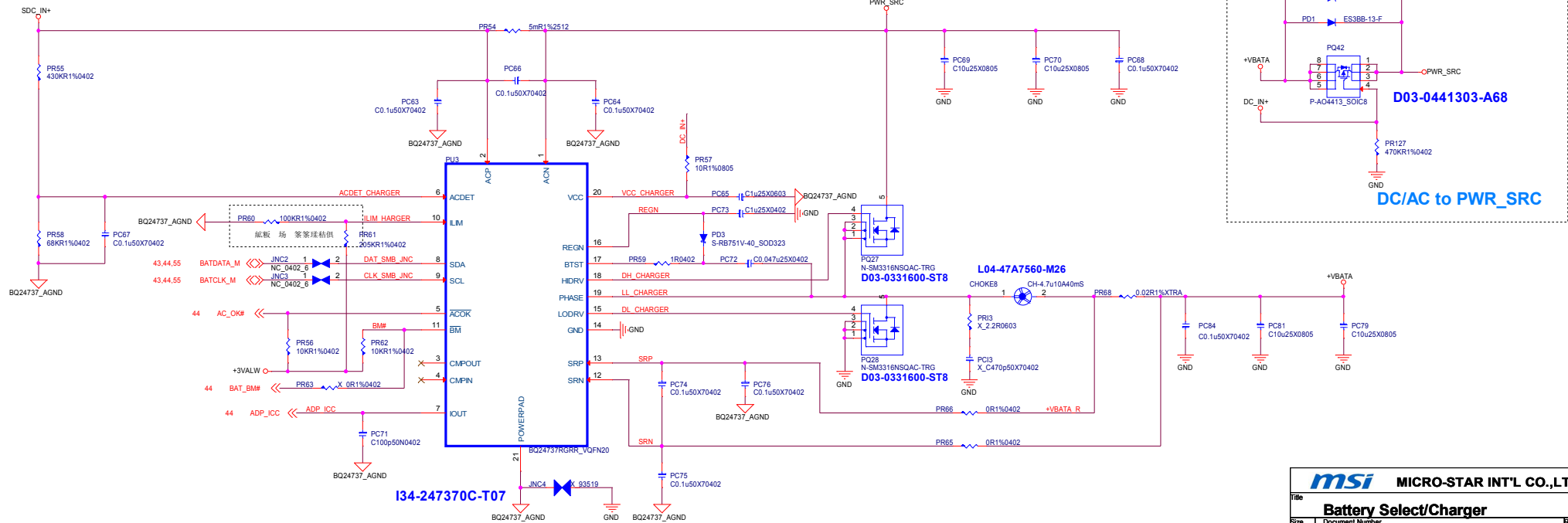


Battery Select/Charger

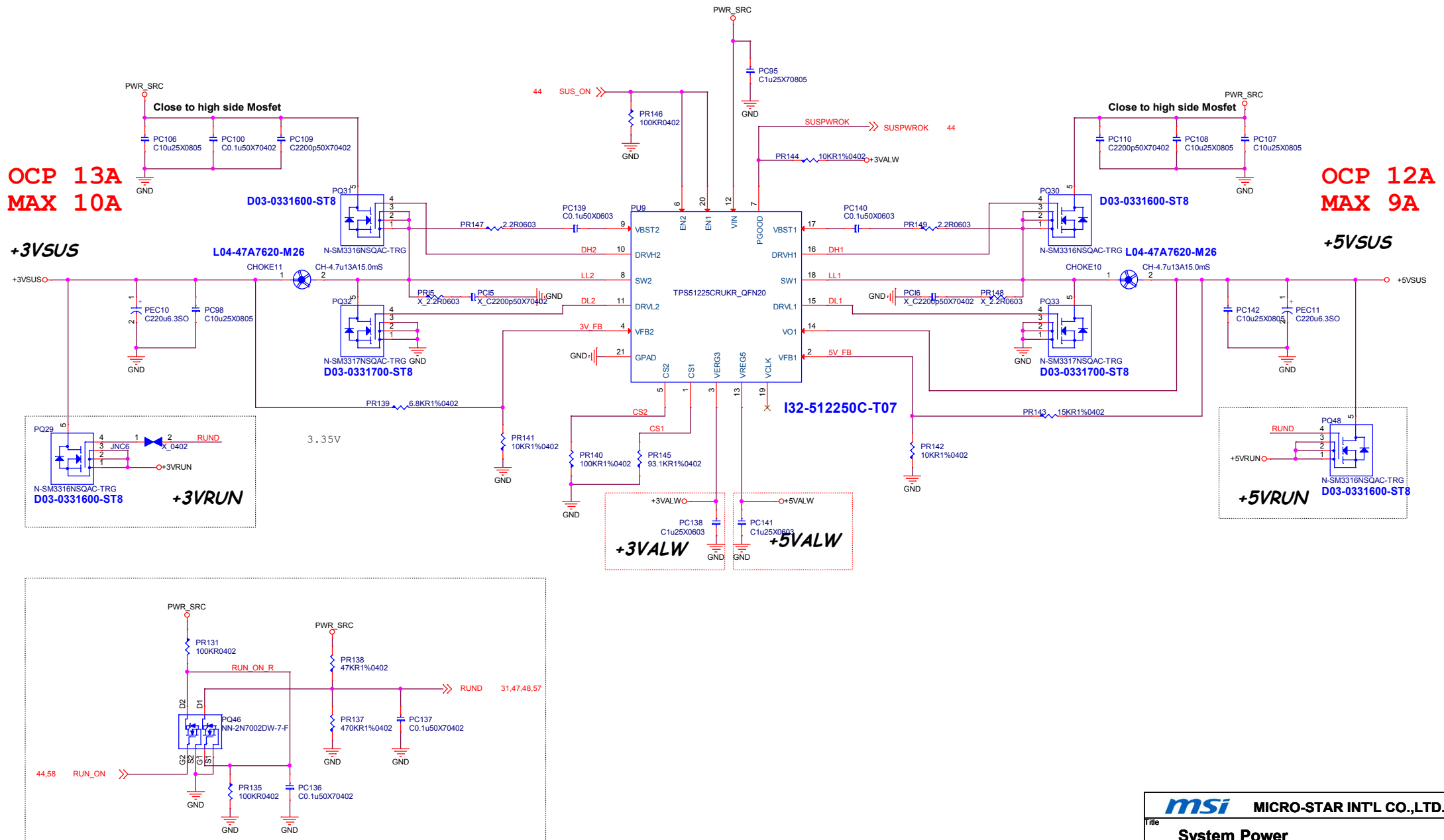
Battery Select



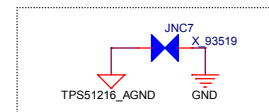
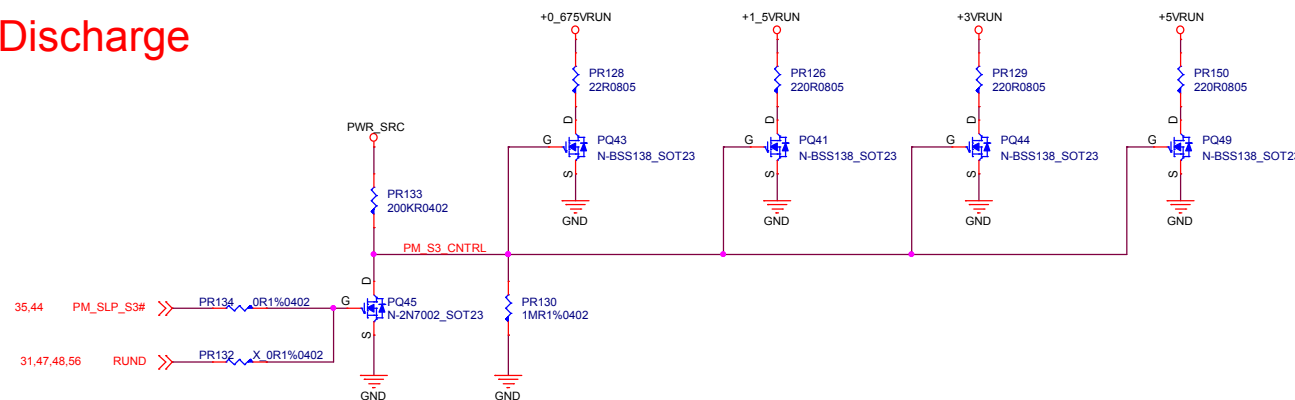
Battery Charger



System Power

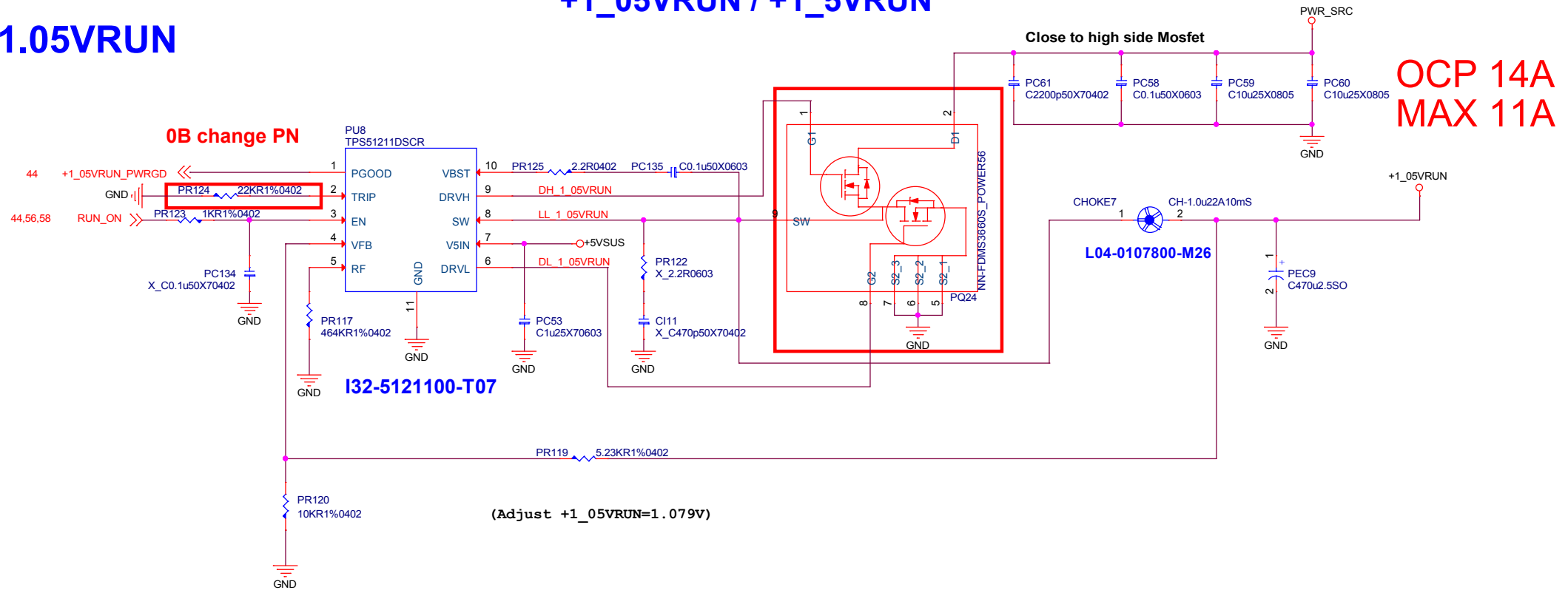


+1.35VDIMM & +0.675VRUN

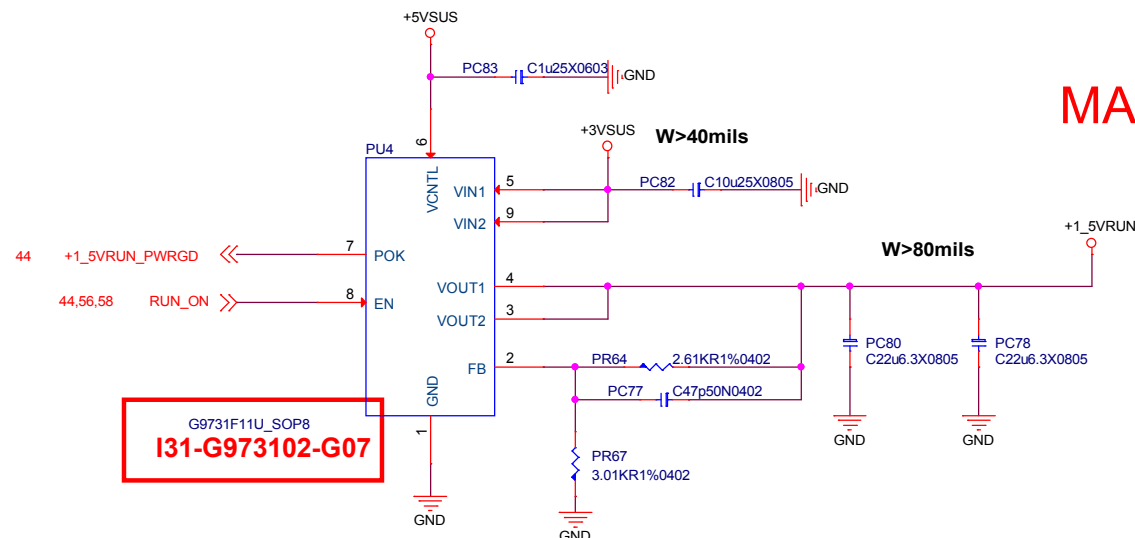


+1.05VRUN

+1_05VRUN / +1_5VRUN



+1.5VRUN

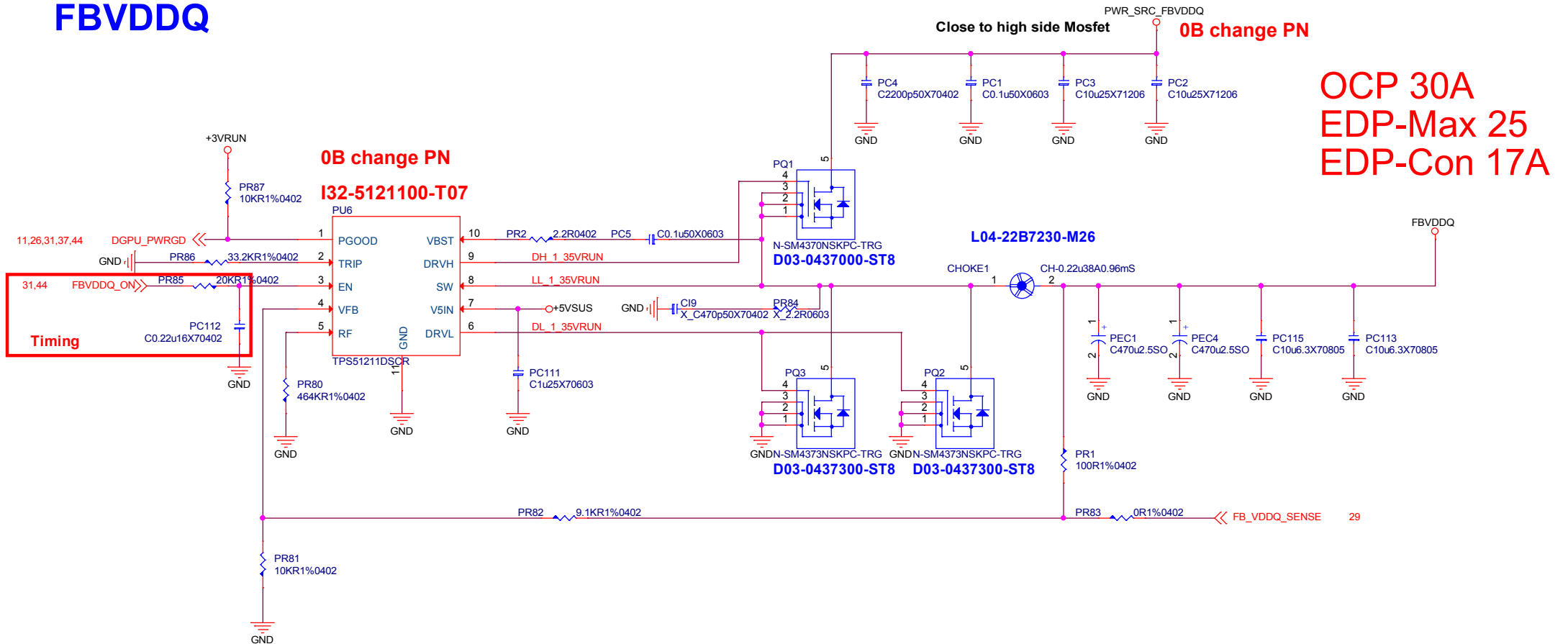


MAX 2A

msi MICRO-STAR INT'L CO.,LTD.	
Title	
+1_05VRUN / +1_5VRUN	
Size	Document Number
	MS-16H5
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DGPU POWER FBVDDQ

FBVDDQ

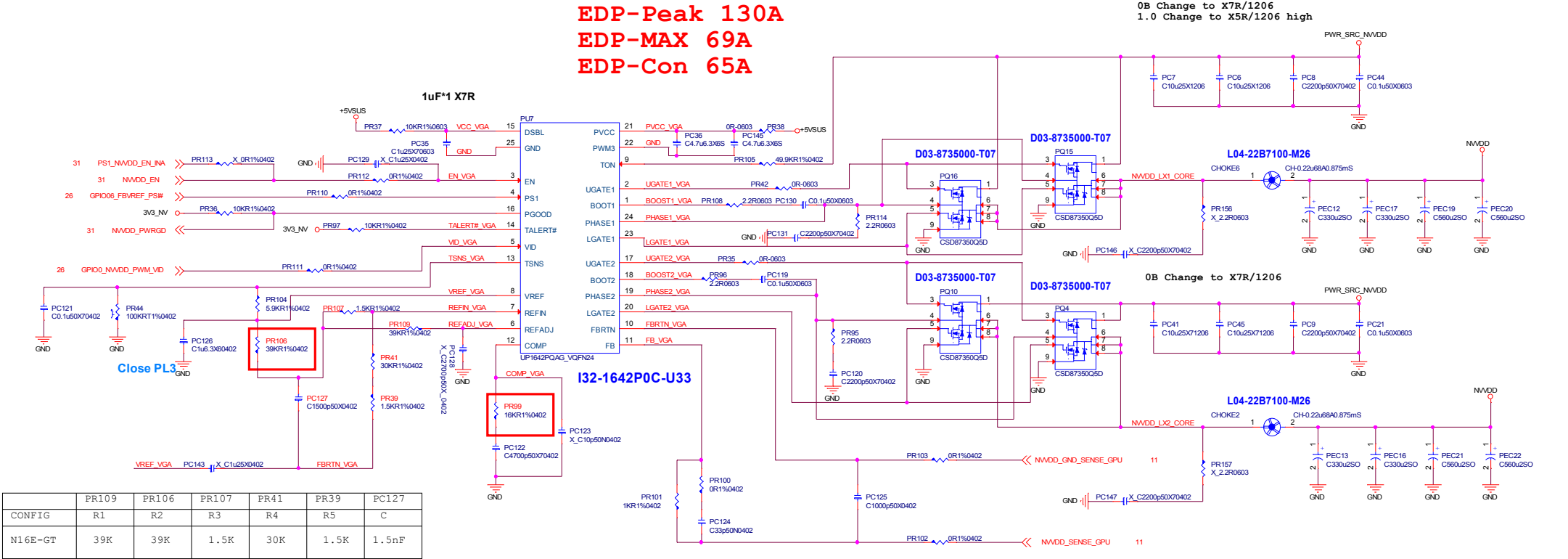


DGPU POWER NVVDD

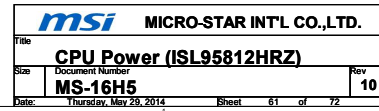
DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 130A
EDP-MAX 69A
EDP-Con 65A



MAX 95A
TDC 27A



EMI/ Impedance

Impedance Connector No PN

40 ohm



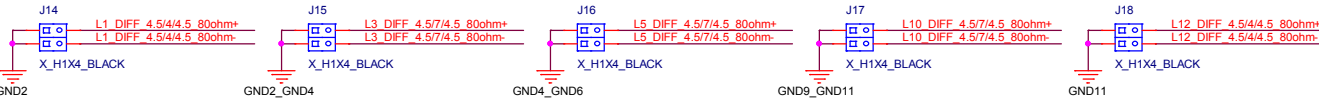
45 ohm



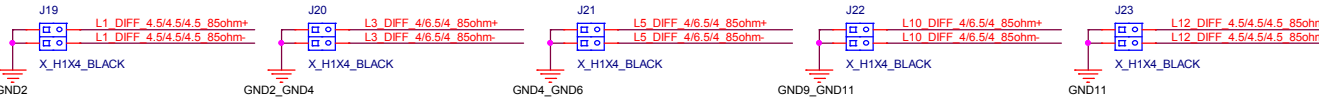
50 ohm



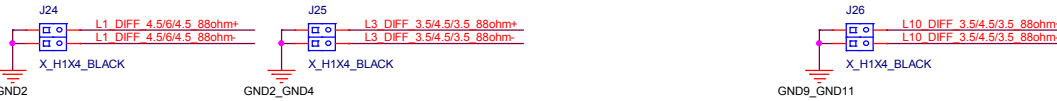
80 ohm



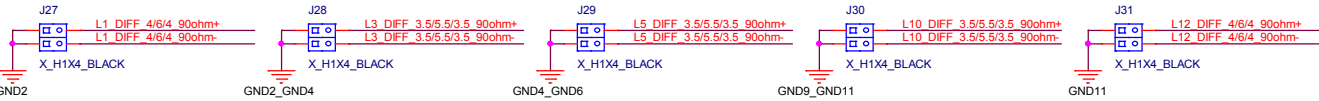
85 ohm



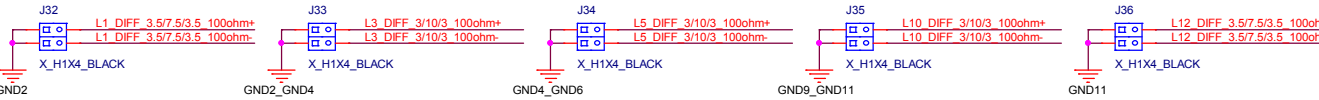
88 ohm



90 ohm



100 ohm

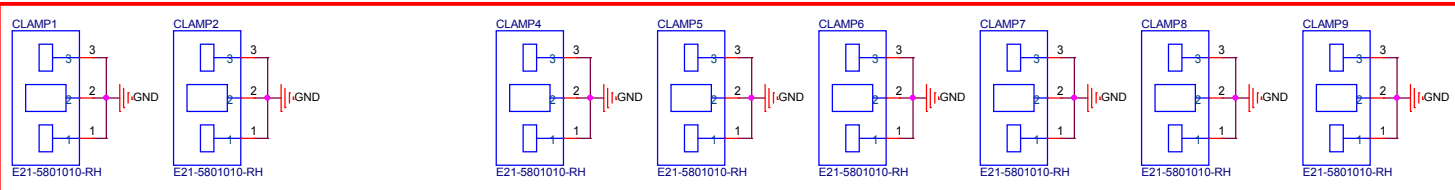
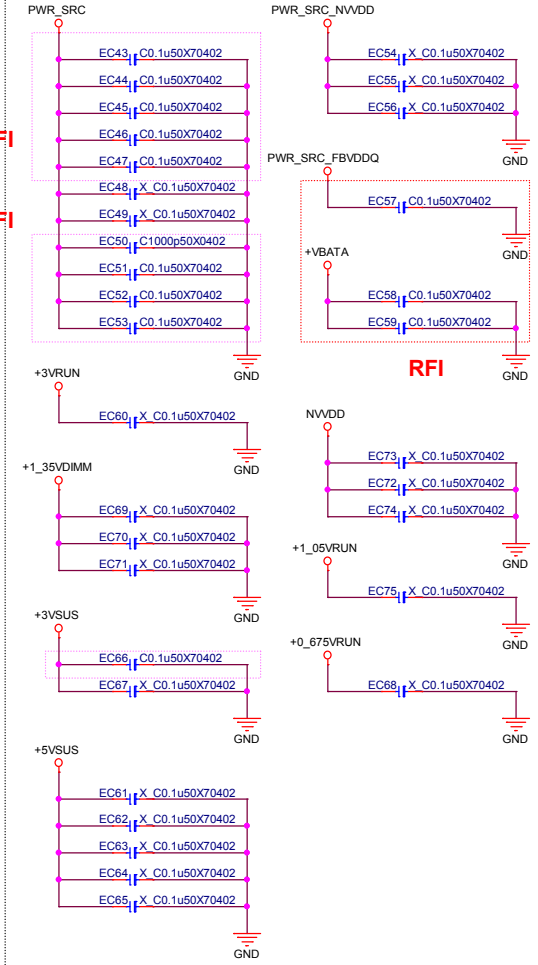


EMI

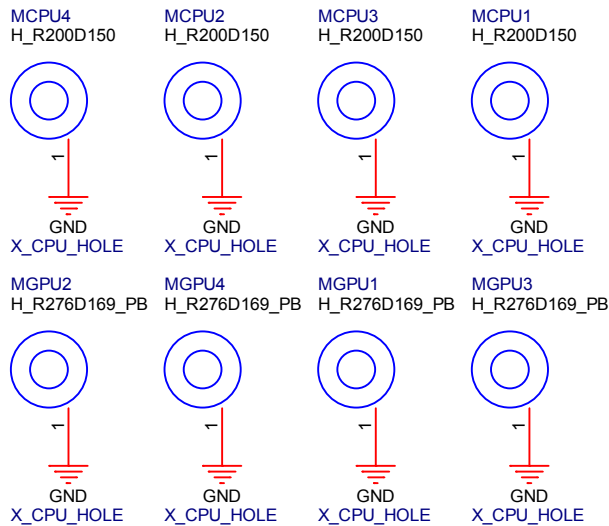
RFI

RFI

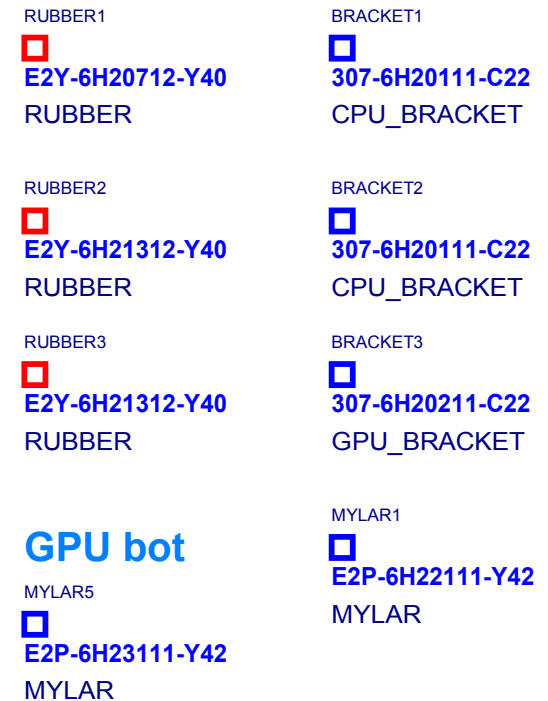
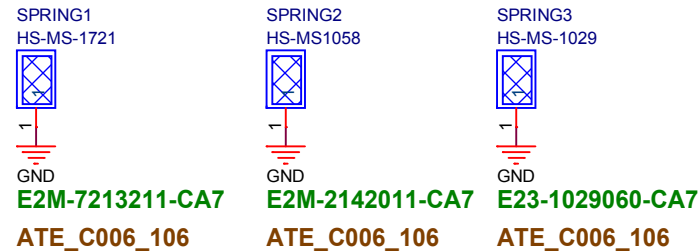
RFI



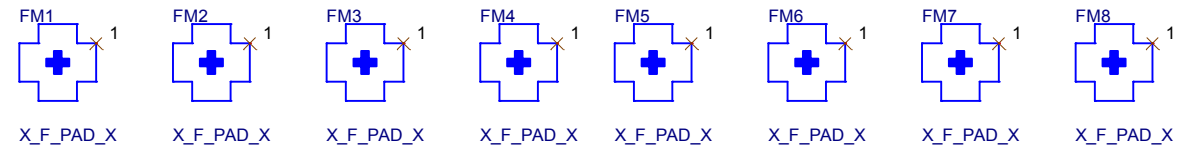
CPU/GPU Holes



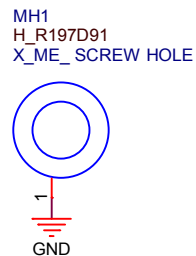
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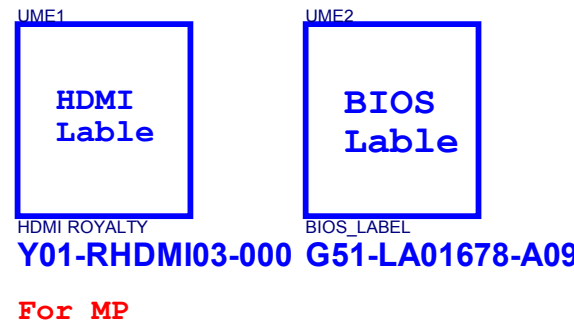
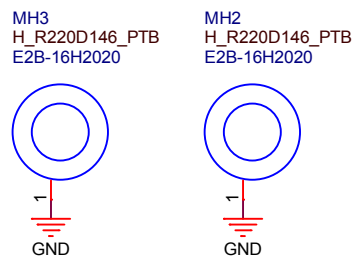
GPU bot



Fan Hole



SSD Stand off

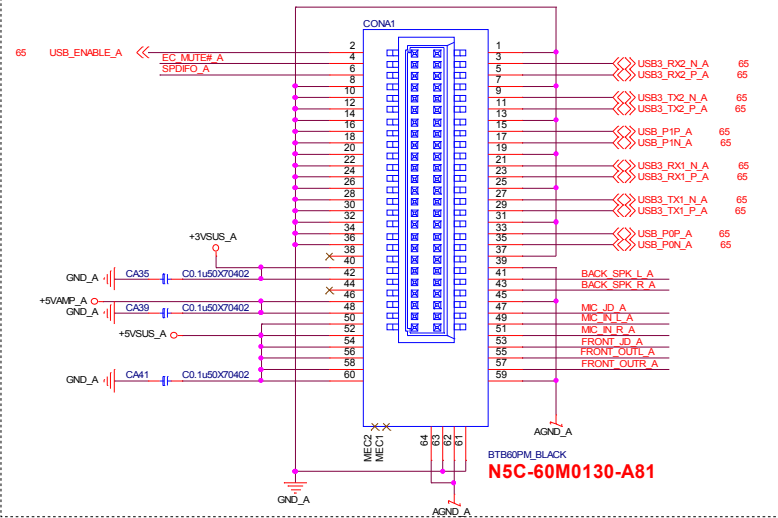


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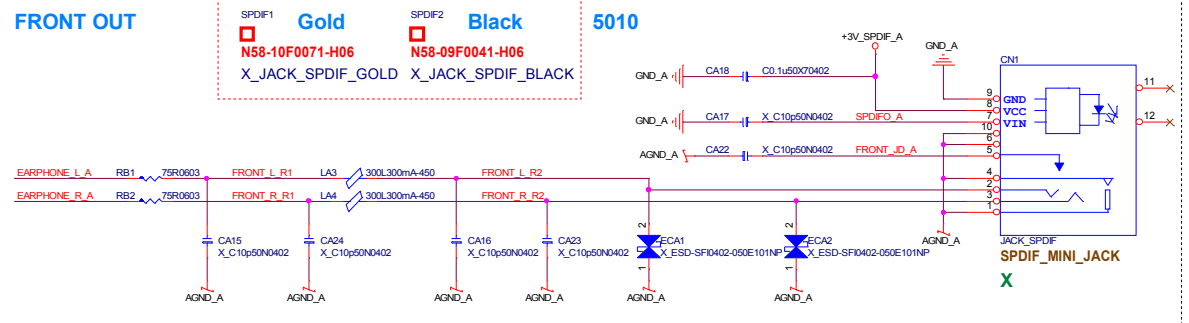
Title		
Screw/ME		
Size	Document Number	Rev
	MS-16H5	10
Date:	Thursday, May 29, 2014	Sheet 63 of 72

16H5-A Board (Audio CONN)

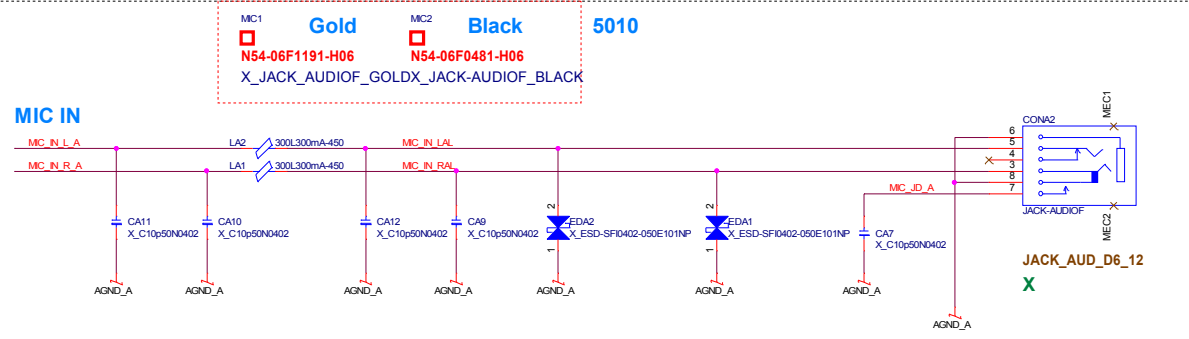
BTB Connector From MB CONN Pin Current Capability : 0.5A/Pin



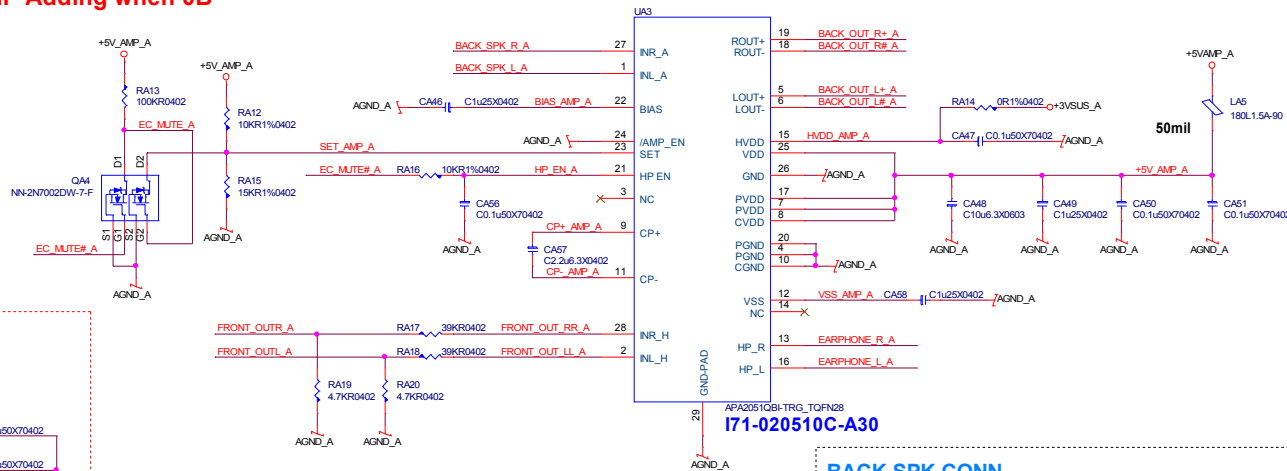
FRONT OUT



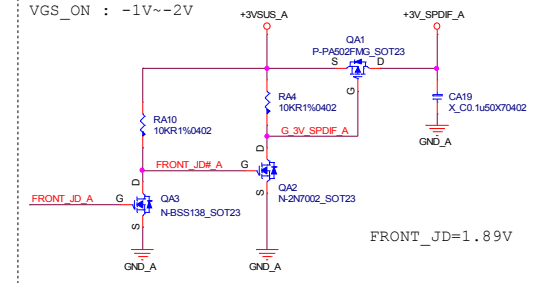
MIC IN



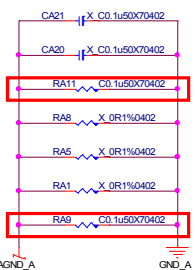
AMP Adding when 0B



SPDIF Power



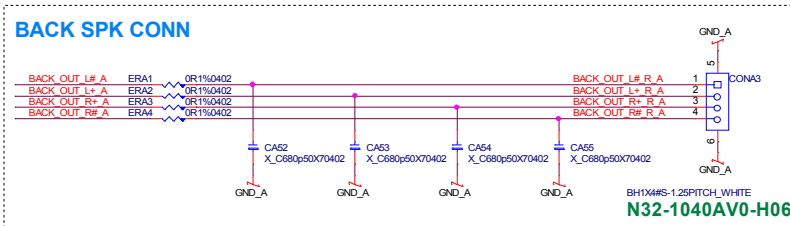
EMI



Change to Cap

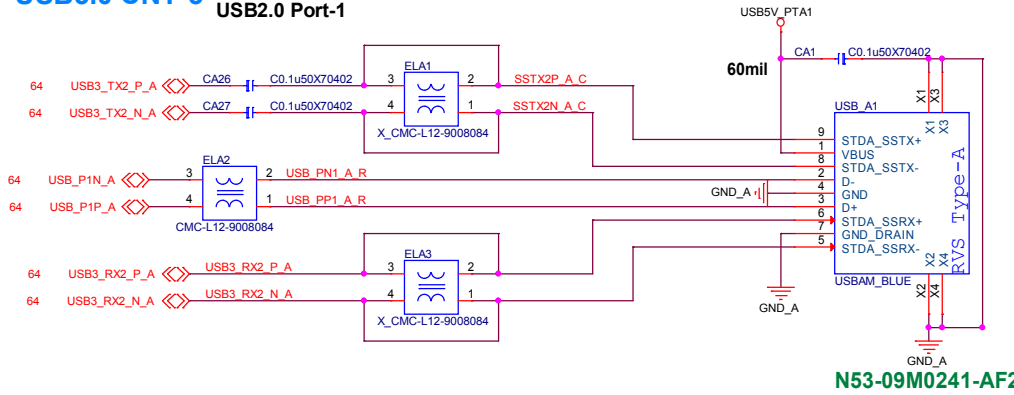
Change to Cap

BACK SPK CONN

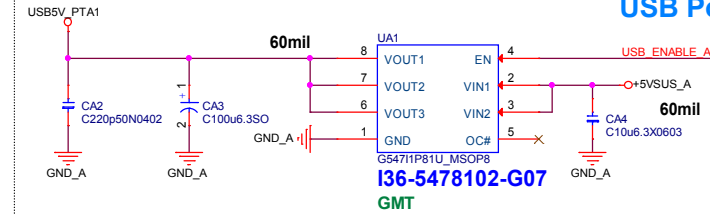


[A] USB3.0 CNT-2/-3

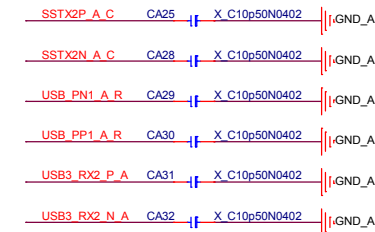
USB3.0 CNT-3 USB3.0 Port-2 USB2.0 Port-1



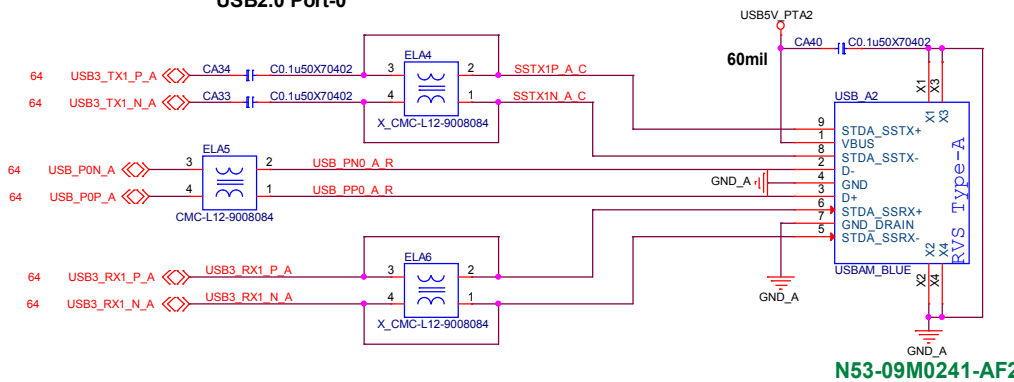
USB Power Switch



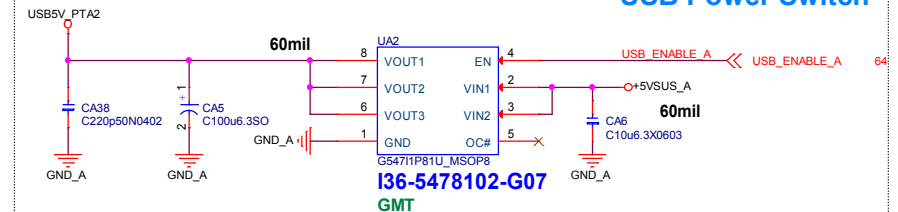
EMI



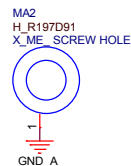
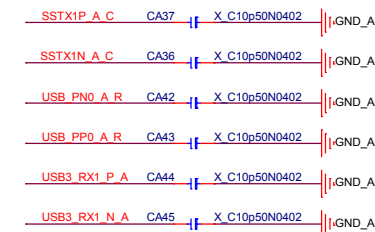
USB3.0 CNT-4 USB3.0 Port-1 USB2.0 Port-0



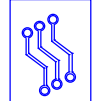
USB Power Switch



EMI



PCBA1



PF0-16H5A10-H73

PF0-16H5A10-H73

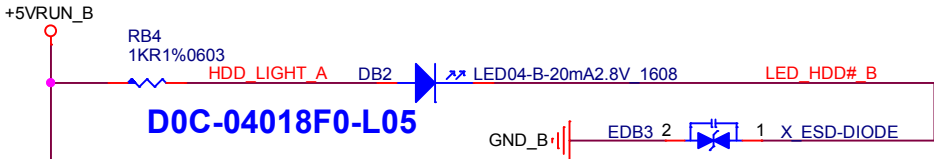
Hannstar: PF0-16H5A10-H73
TRIPOD: PF0-16H5A10-T53

MYLARA1	MYLARA2
E2P-6H22812-G40	E2P-6H22311-G40
MYLAR	MYLAR

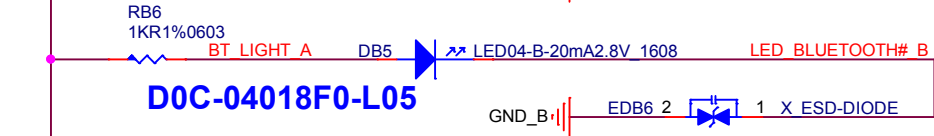
16H5-B Board (LED Board)

LED

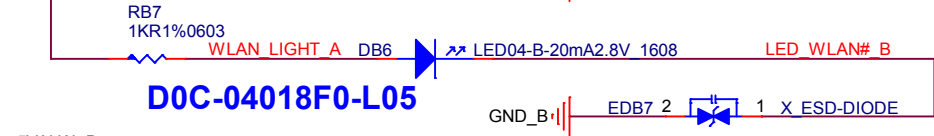
BLUE
(HDD)



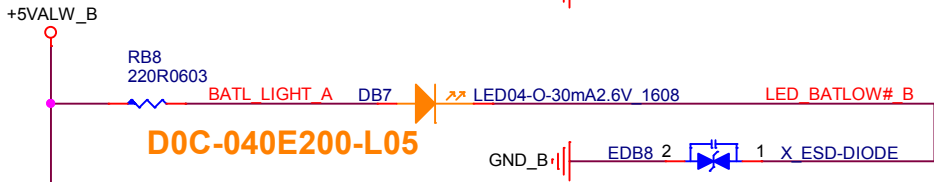
BLUE
(BT)



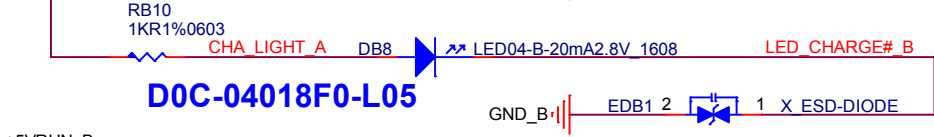
BLUE
(WLAN)



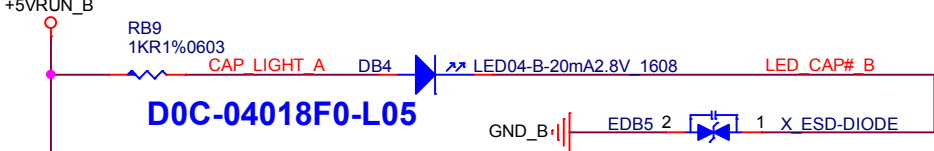
ORANGE
(BATLOW)



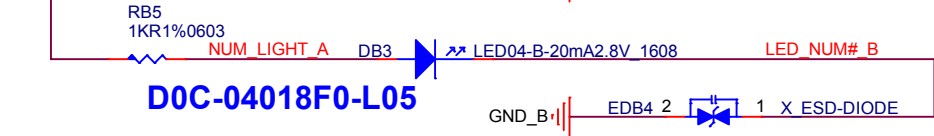
BLUE
(CHARGE)



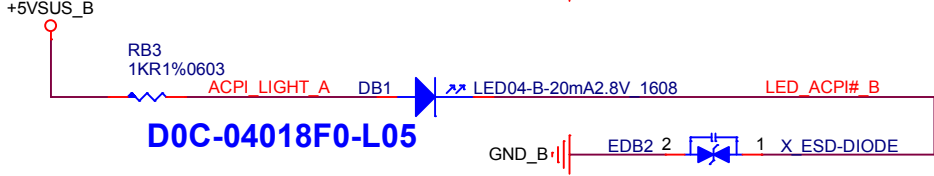
BLUE
(CAP)



BLUE
(NUM)

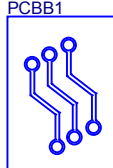
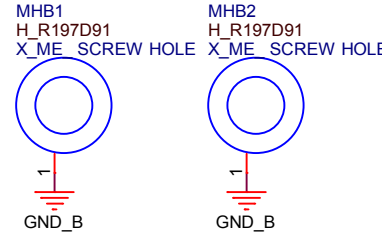
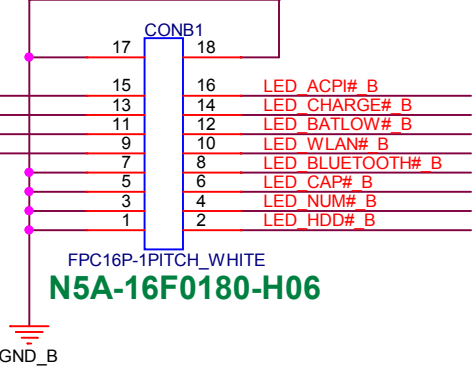


BLUE
(ACPI)



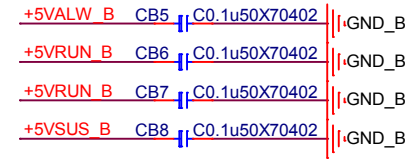
Connector


Same Side



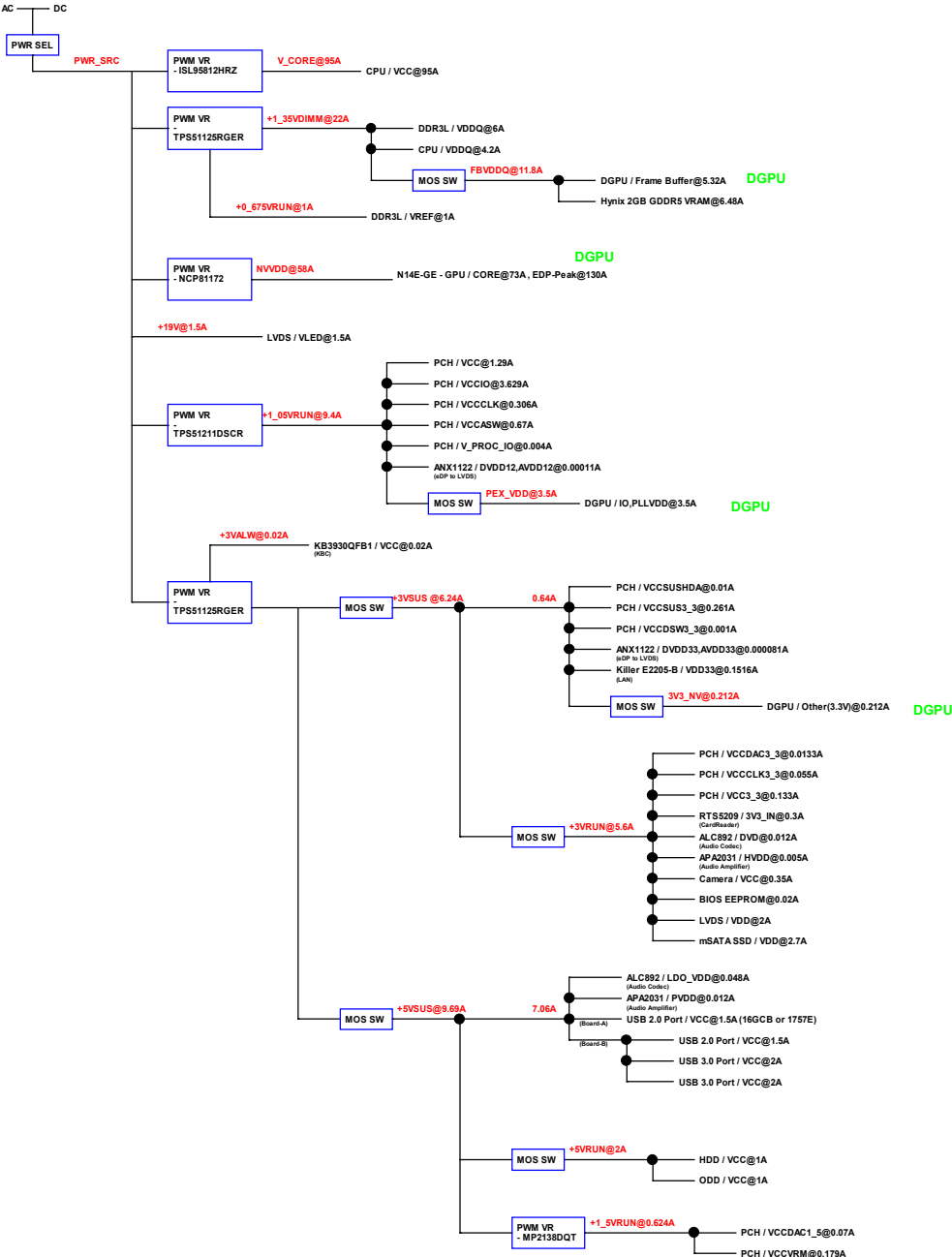
PF0-16H5B10-H73
PF0-16H5B10-H73

Hannstar: PF0-16H5B10-H73
TRIPOD: PF0-16H5B10-T53

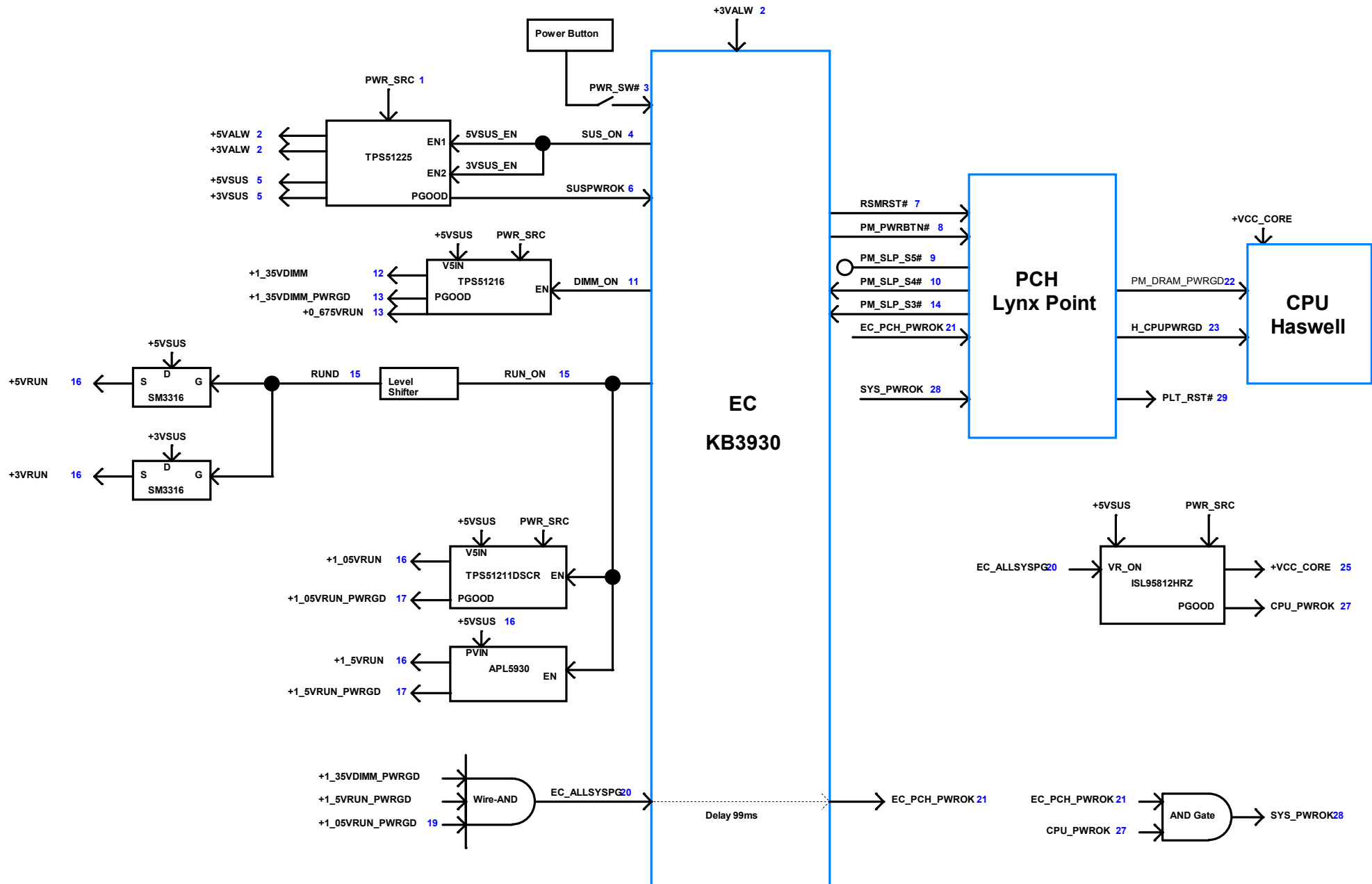


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LED Board			
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MS-16H5 Power Delivery Chart

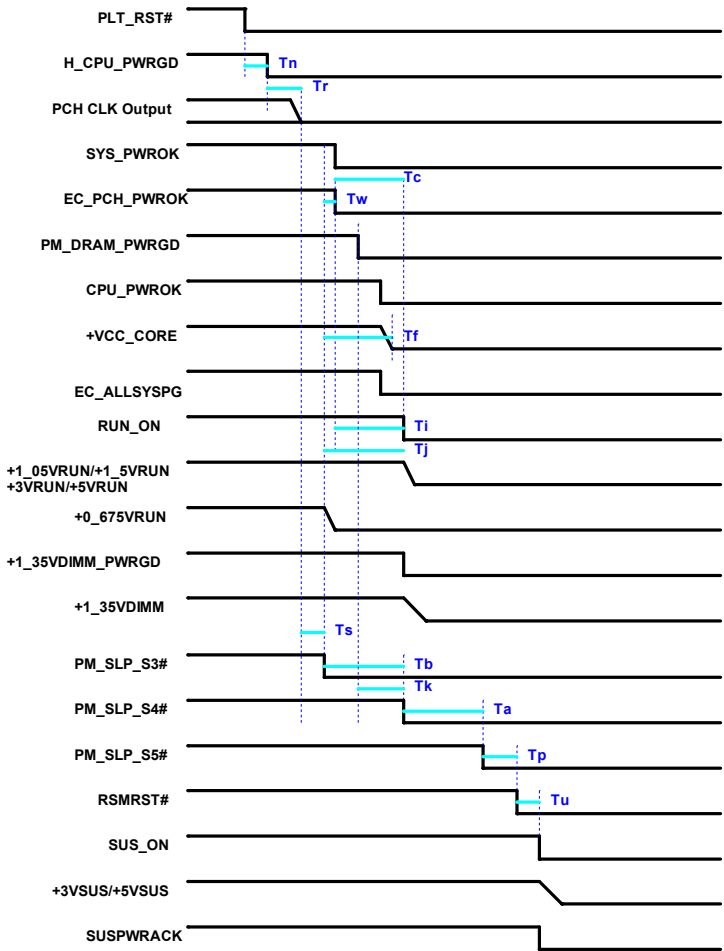


MS-16H5 Power on Block Diagram



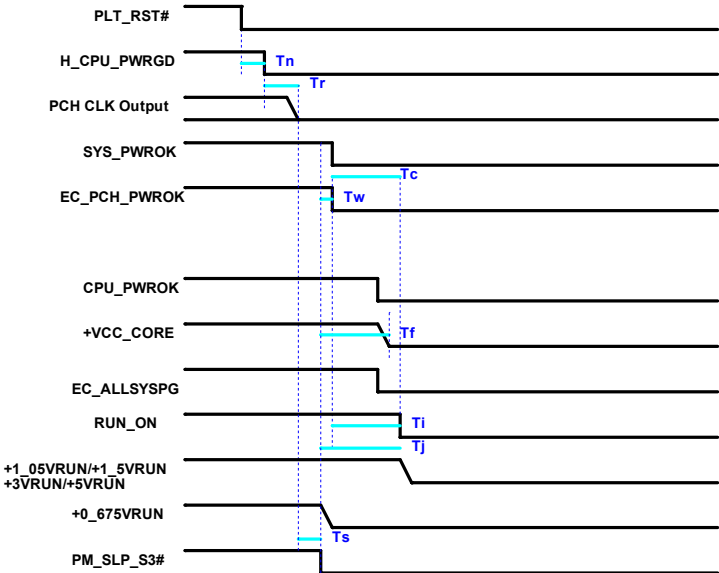
Power down Sequence

S0 -> G3



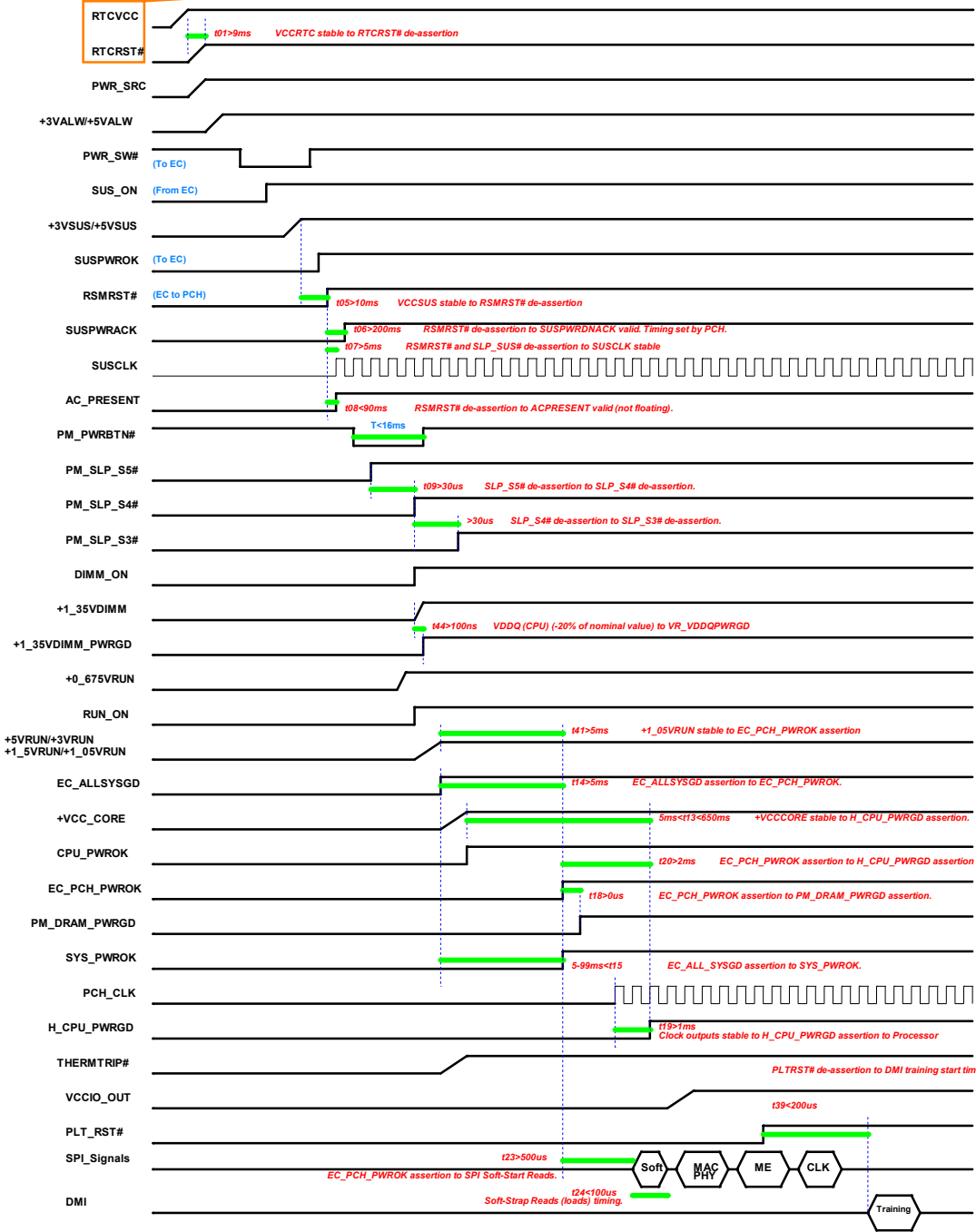
	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3

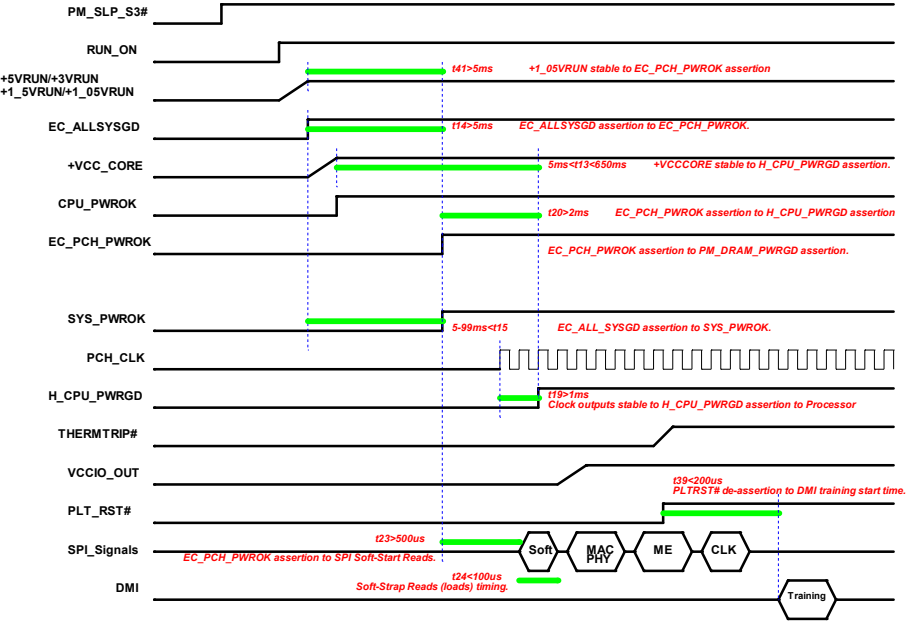


Power on Sequence


G3 -> S0



S3-> S0



History

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